

FIG. 1 is a block diagram of a system 100. The system 100 includes a processor 110, a memory 115, a network interface 120, a storage device 125, and a user interface 130. The processor 110 is connected to the memory 115, the network interface 120, the storage device 125, and the user interface 130. The network interface 120 is connected to a network 140. The storage device 125 is connected to the processor 110 via a bus 150. The user interface 130 is connected to the processor 110 via a bus 160. The system 100 is configured to execute a program 170. The program 170 is stored in the memory 115. The program 170 is executed by the processor 110. The program 170 is configured to perform a set of operations 180. The operations 180 are performed by the processor 110. The operations 180 are configured to interact with the network interface 120, the storage device 125, and the user interface 130. The operations 180 are configured to receive data from the network interface 120, store data in the storage device 125, and display data to the user interface 130. The operations 180 are configured to perform a set of operations 190. The operations 190 are performed by the processor 110. The operations 190 are configured to interact with the network interface 120, the storage device 125, and the user interface 130. The operations 190 are configured to receive data from the network interface 120, store data in the storage device 125, and display data to the user interface 130.

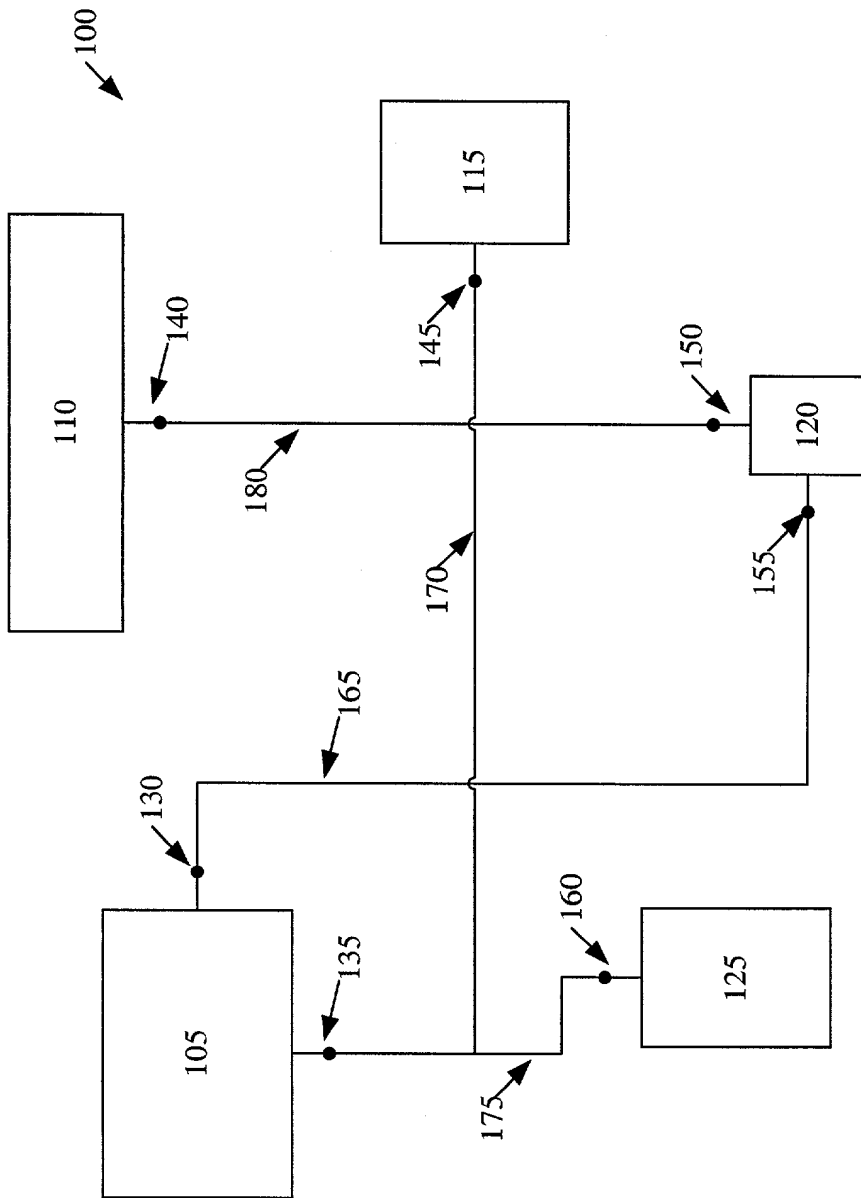


Figure 1

#3

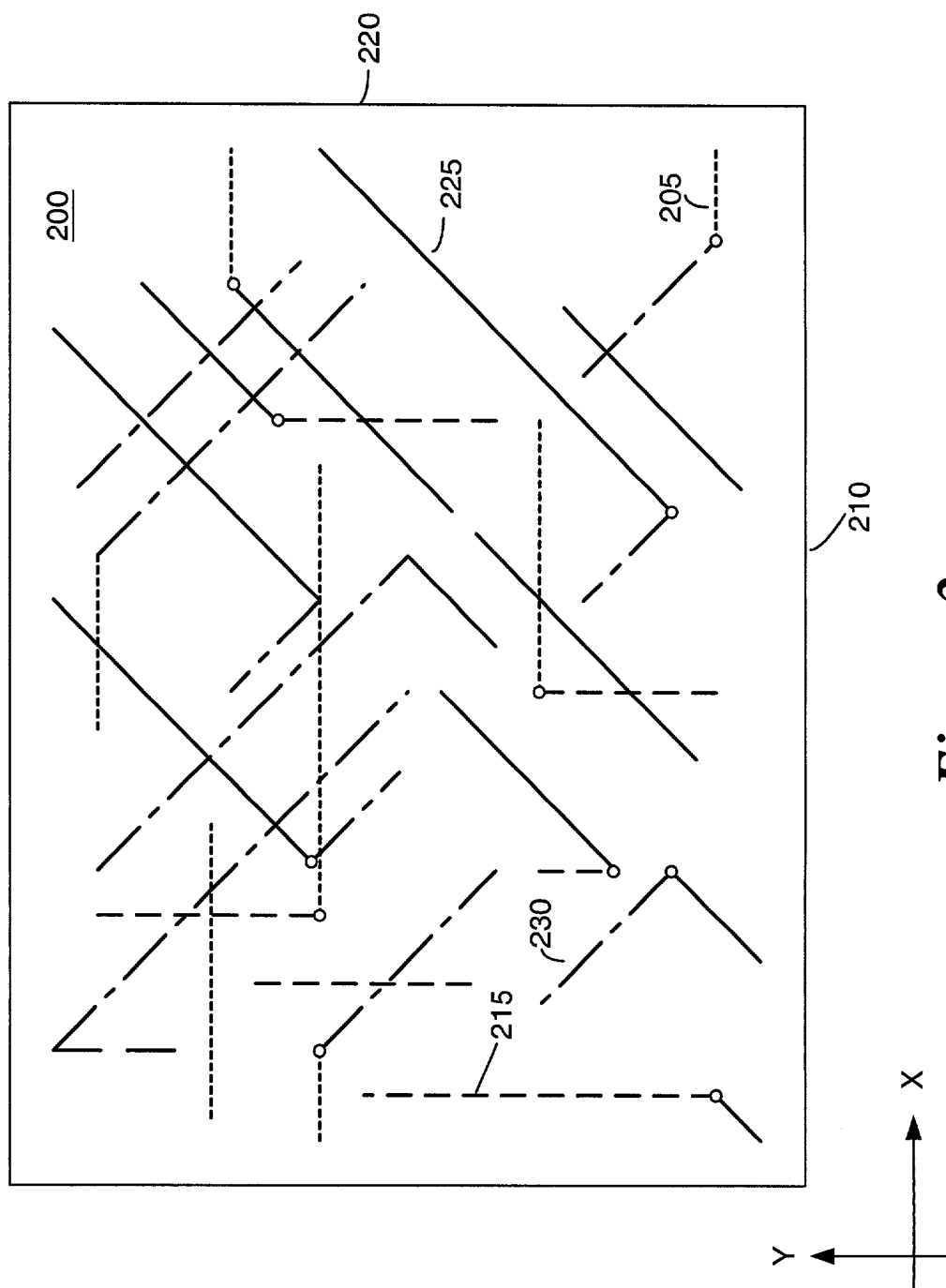


Figure 2

FIG. 3 is a schematic diagram of a multi-layered structure 300. The structure 300 includes a substrate 305, a first layer 310, a second layer 315, a third layer 320, and a fourth layer 325. The layers 310, 315, 320, and 325 are stacked on top of each other, with the substrate 305 at the bottom. The layers 310, 315, 320, and 325 are labeled with arrows pointing to their respective layers.

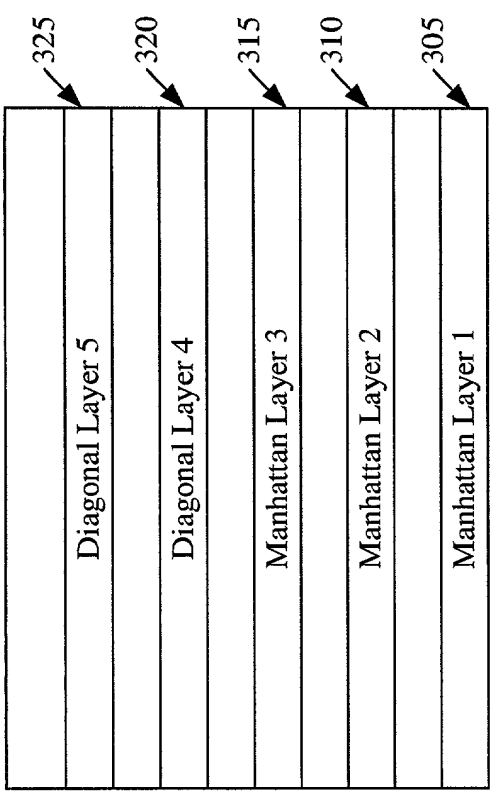


Figure 3



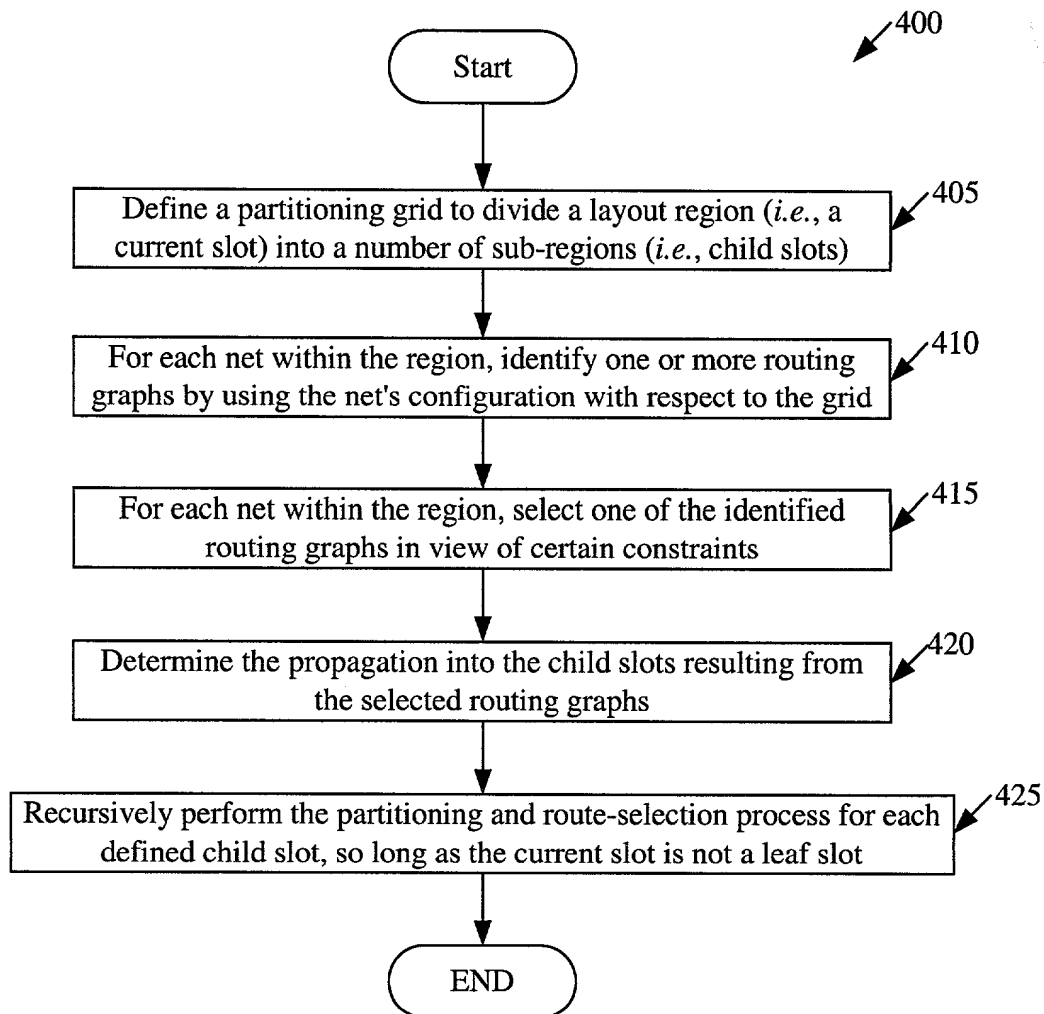


Figure 4

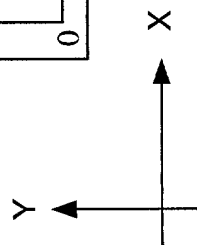
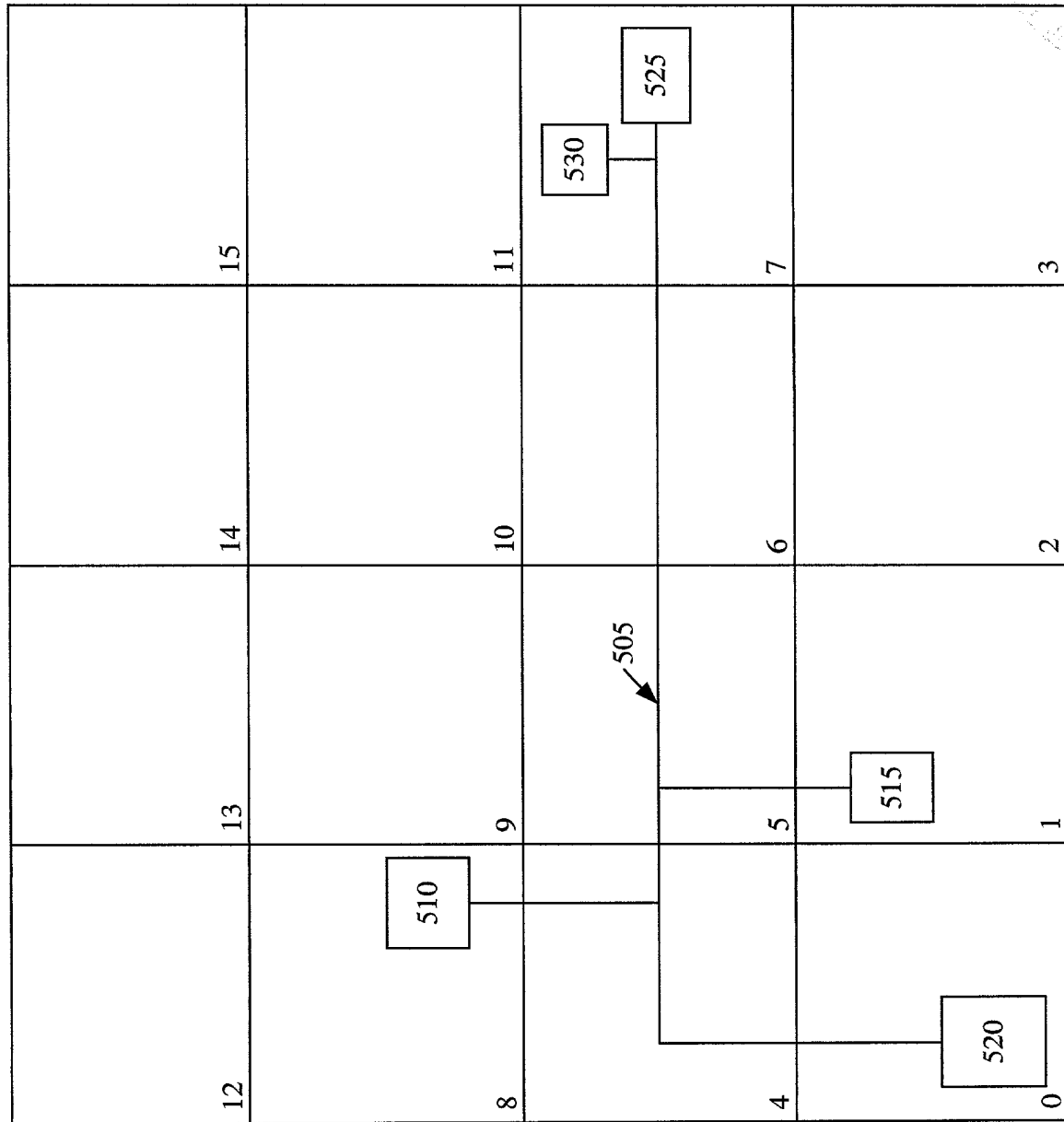


Figure 5

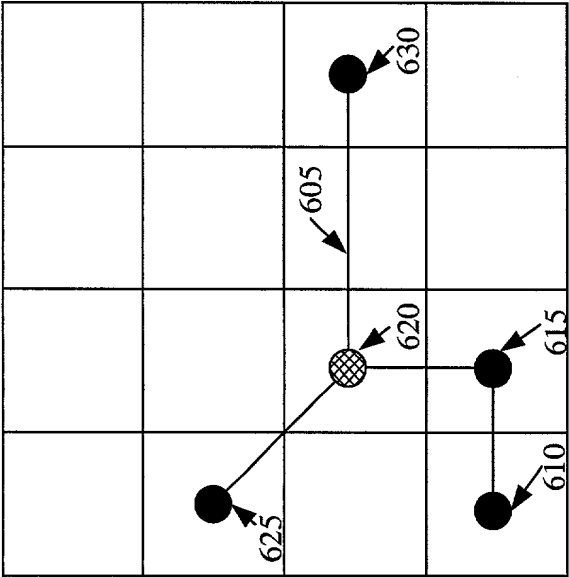


Figure 6

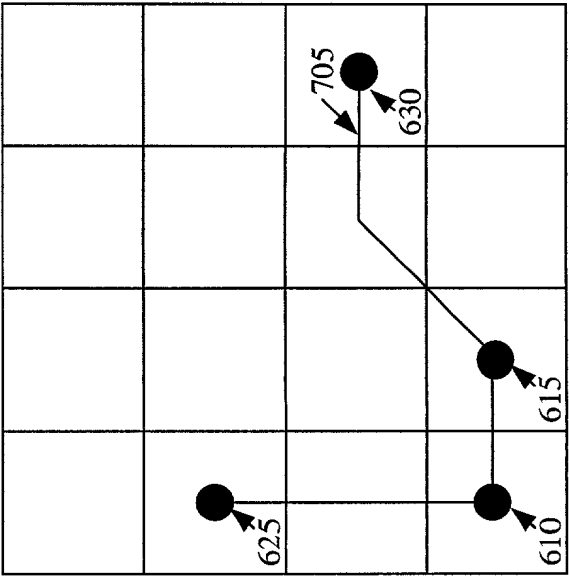


Figure 7

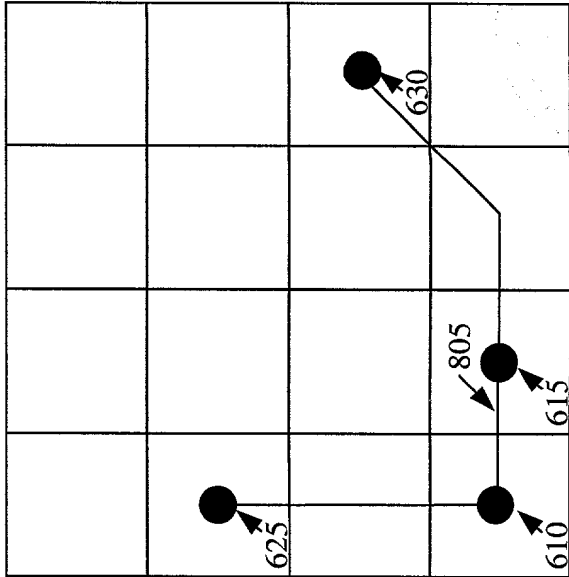


Figure 8

1. The first group of people who are interested in the study of the history of the United States are the people who are interested in the history of the United States.

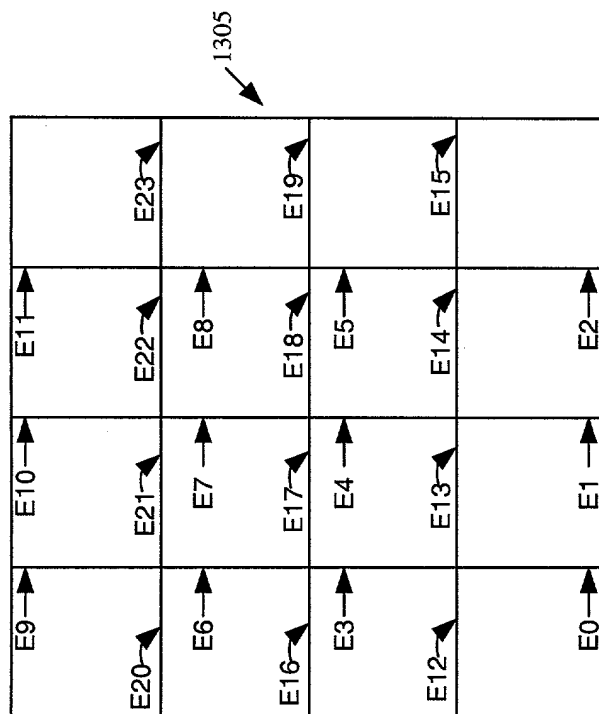


Figure 13

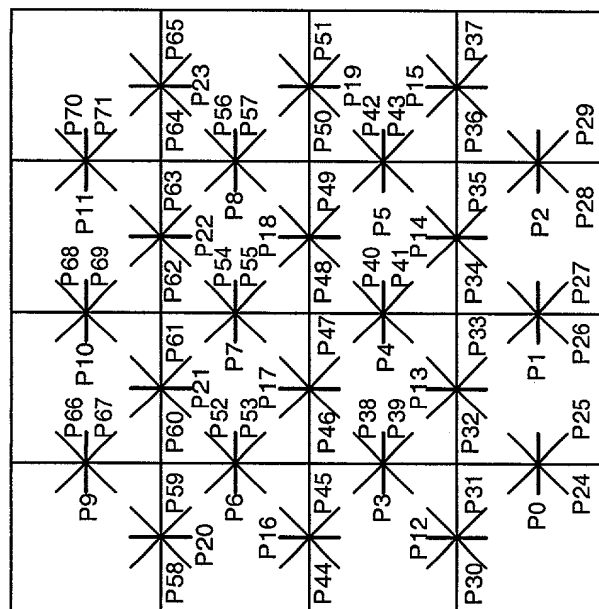


Figure 14

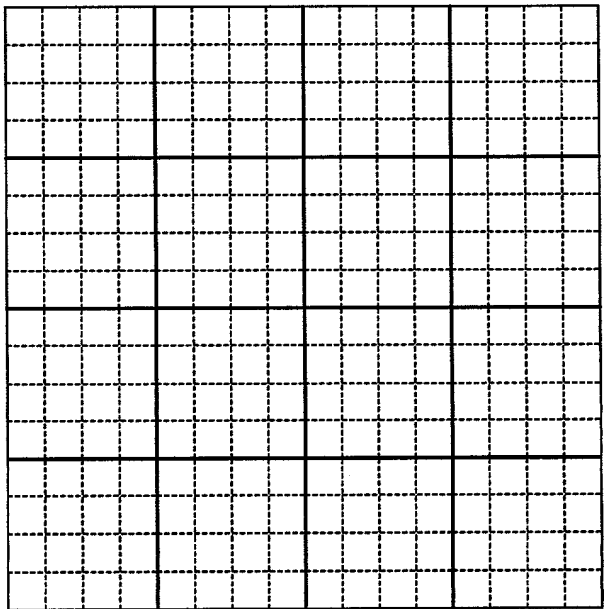


Figure 16

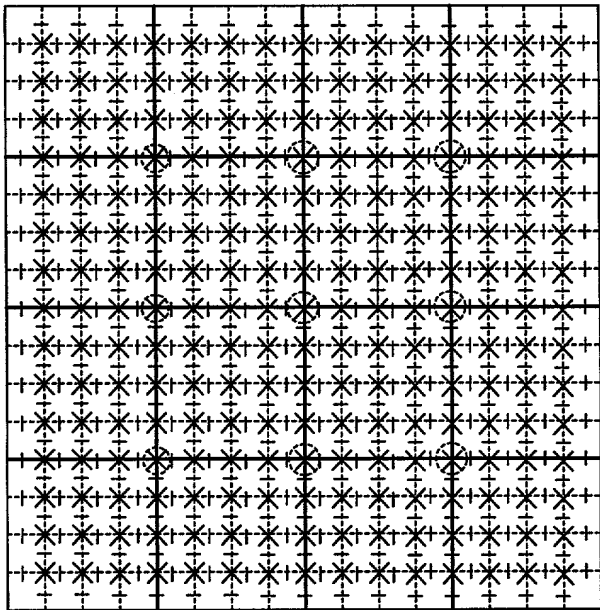


Figure 18



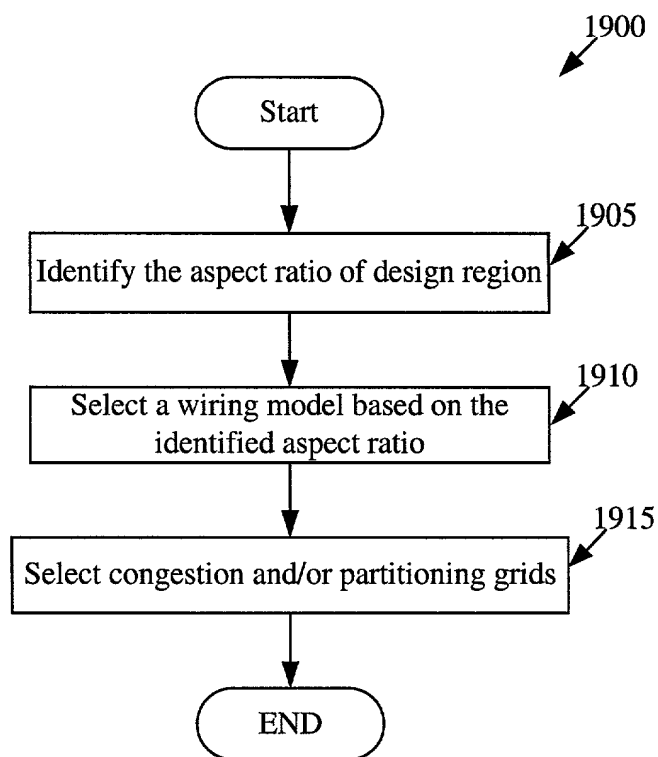


Figure 19

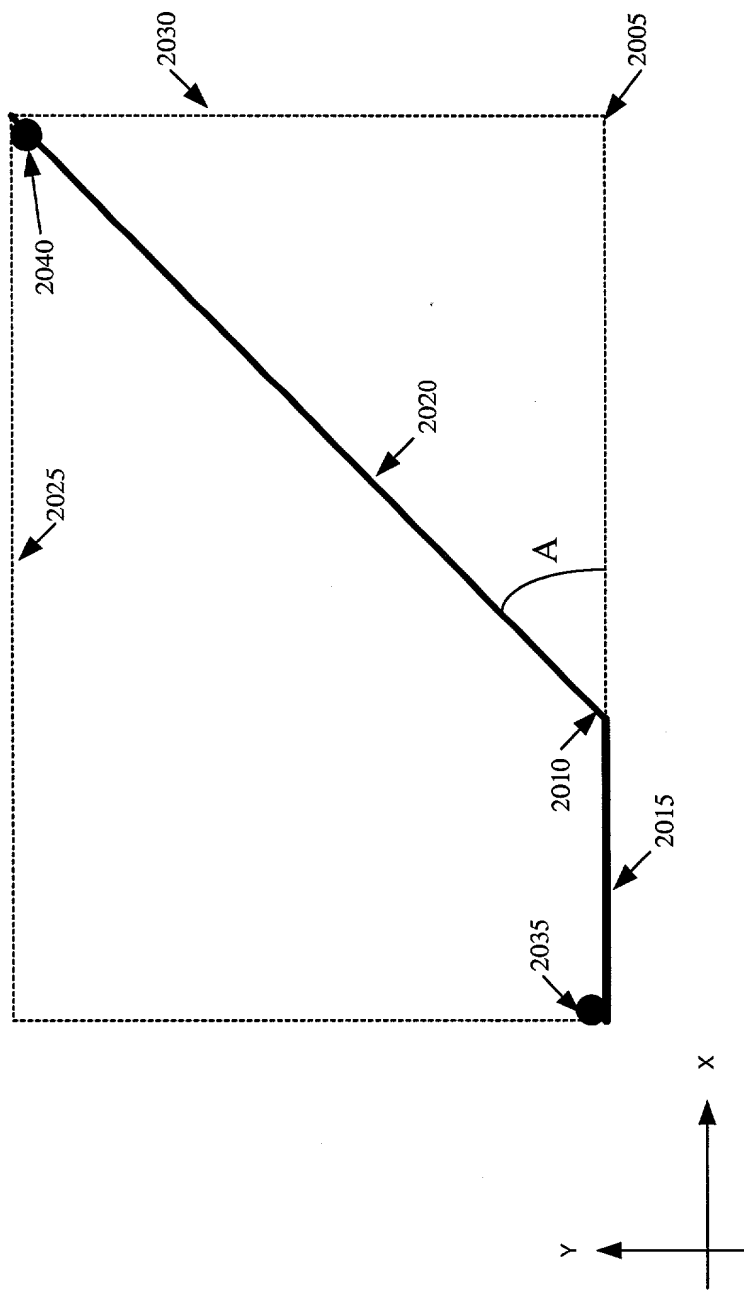


Figure 20

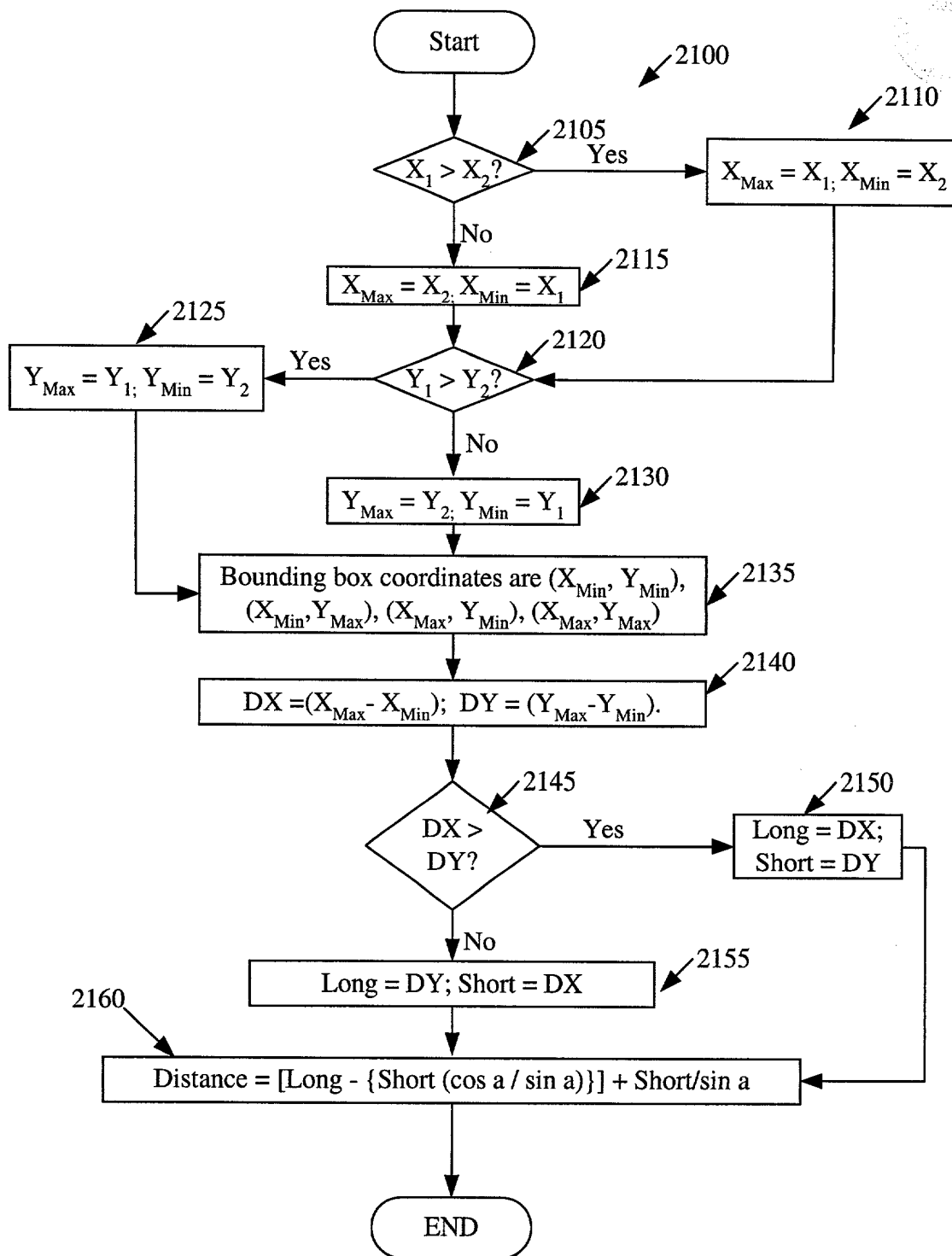


Figure 21

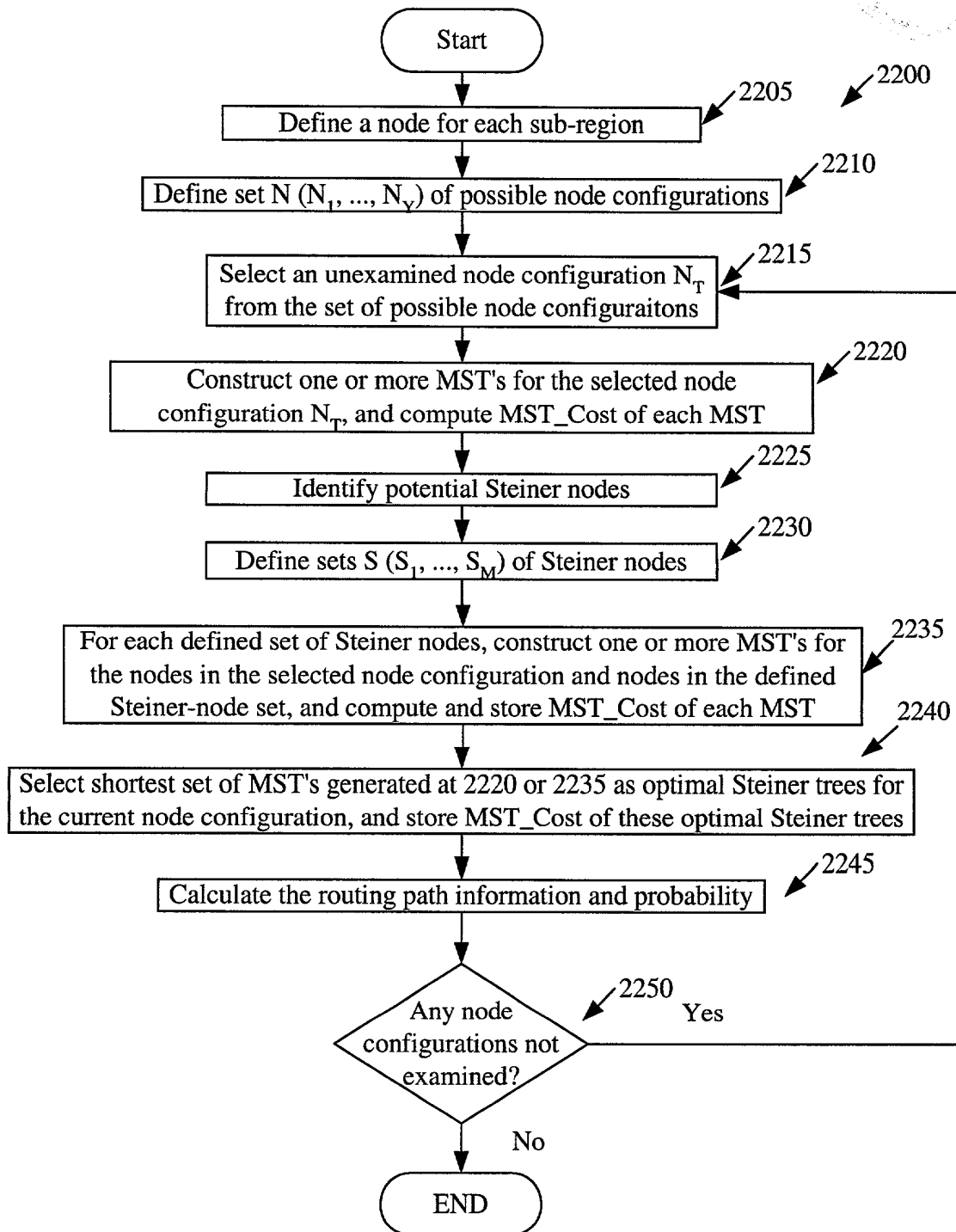


Figure 22

with any of the 16 cells in the 4x4 grid. The cells are numbered 0 to 15, and the arrows point to the cells that are adjacent to the cell in the top-left corner of the grid.

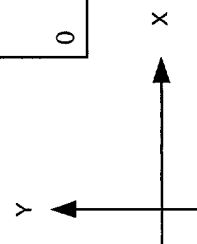
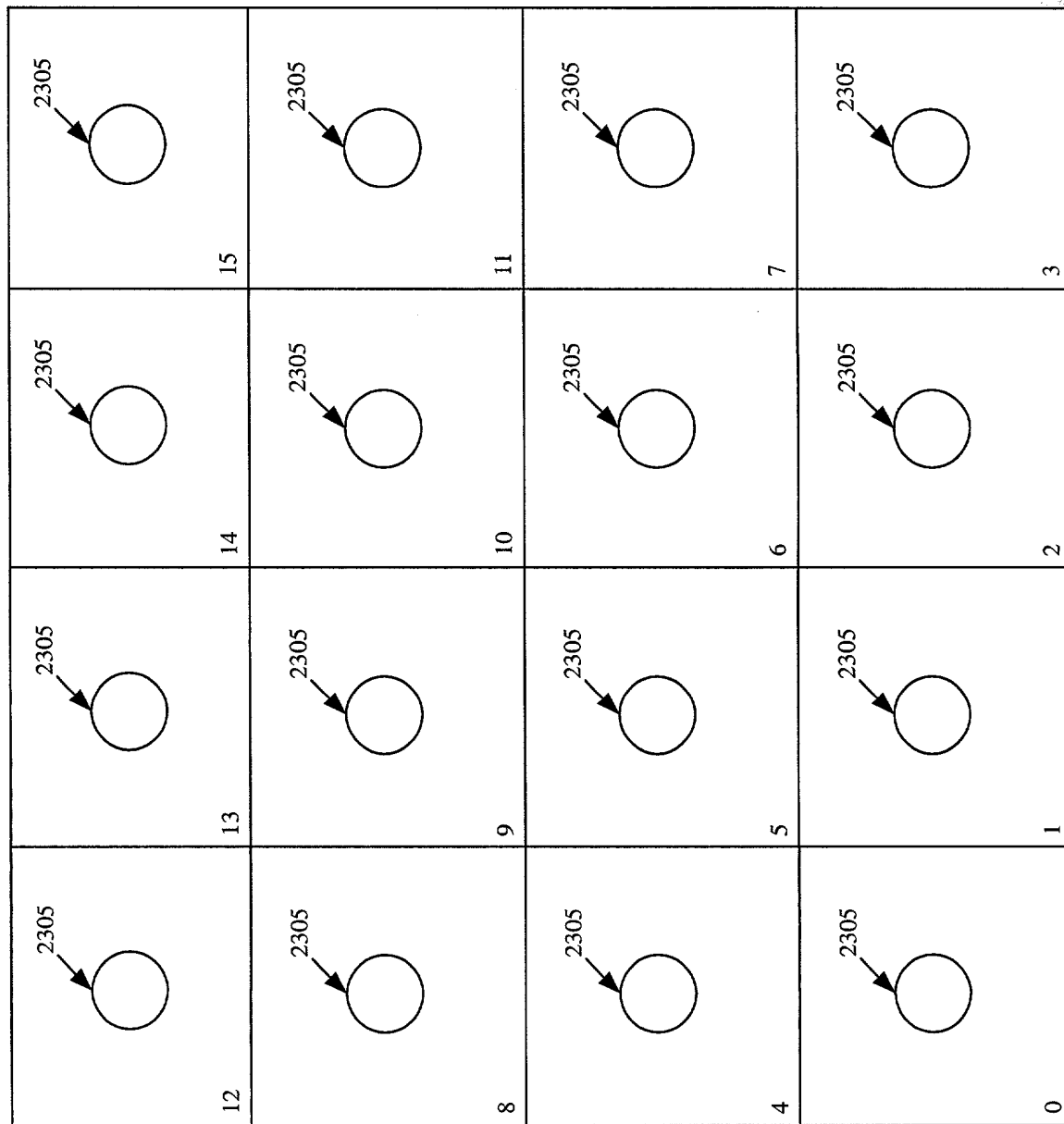


Figure 23

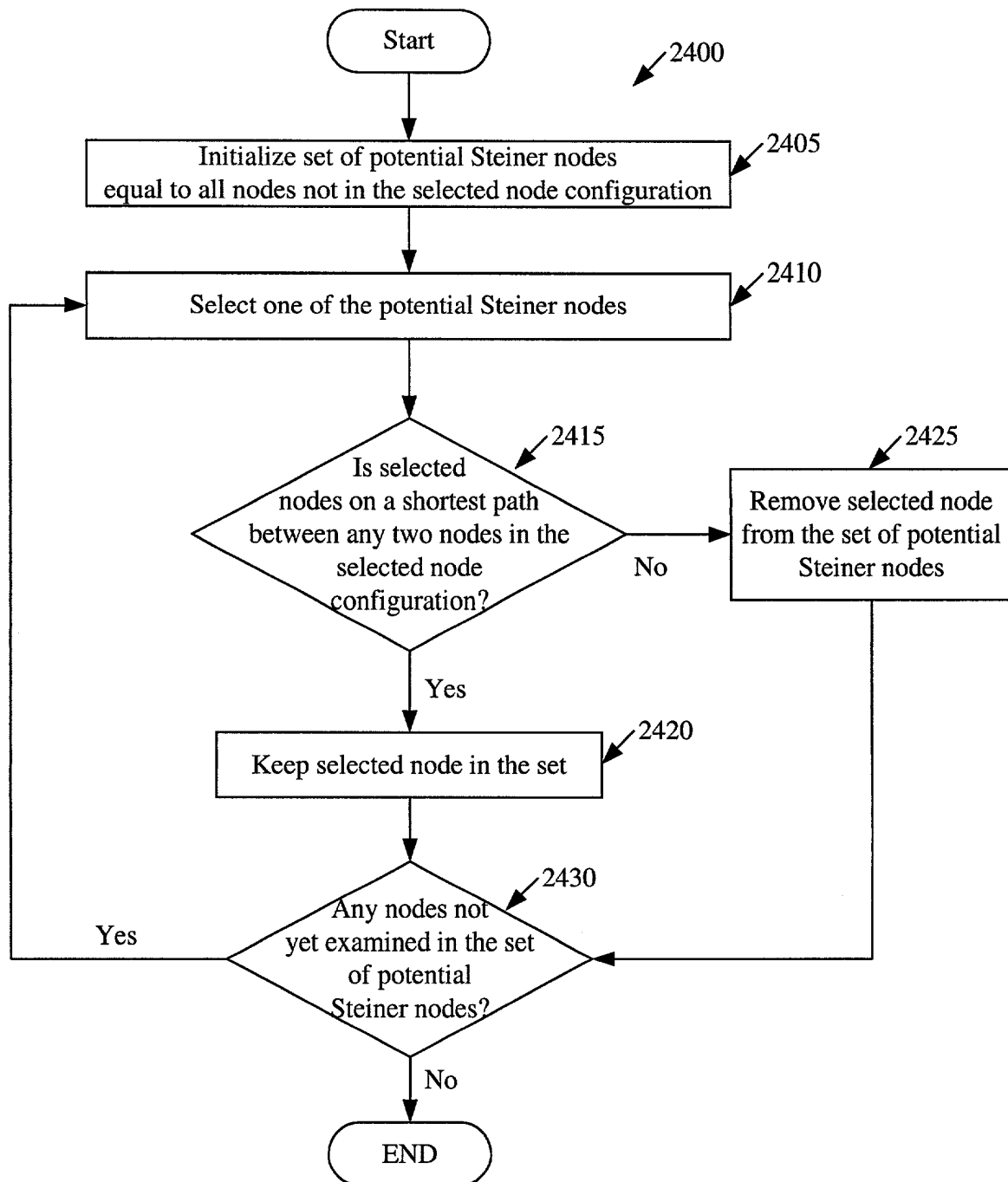


Figure 24

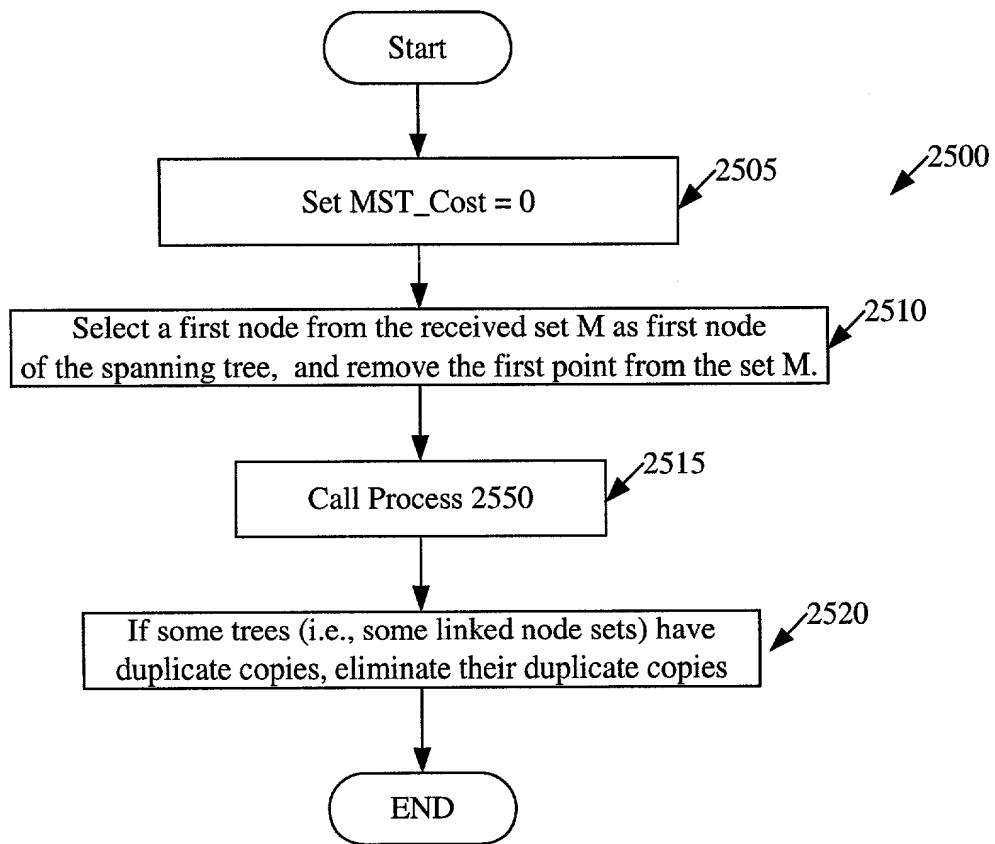


Figure 25A

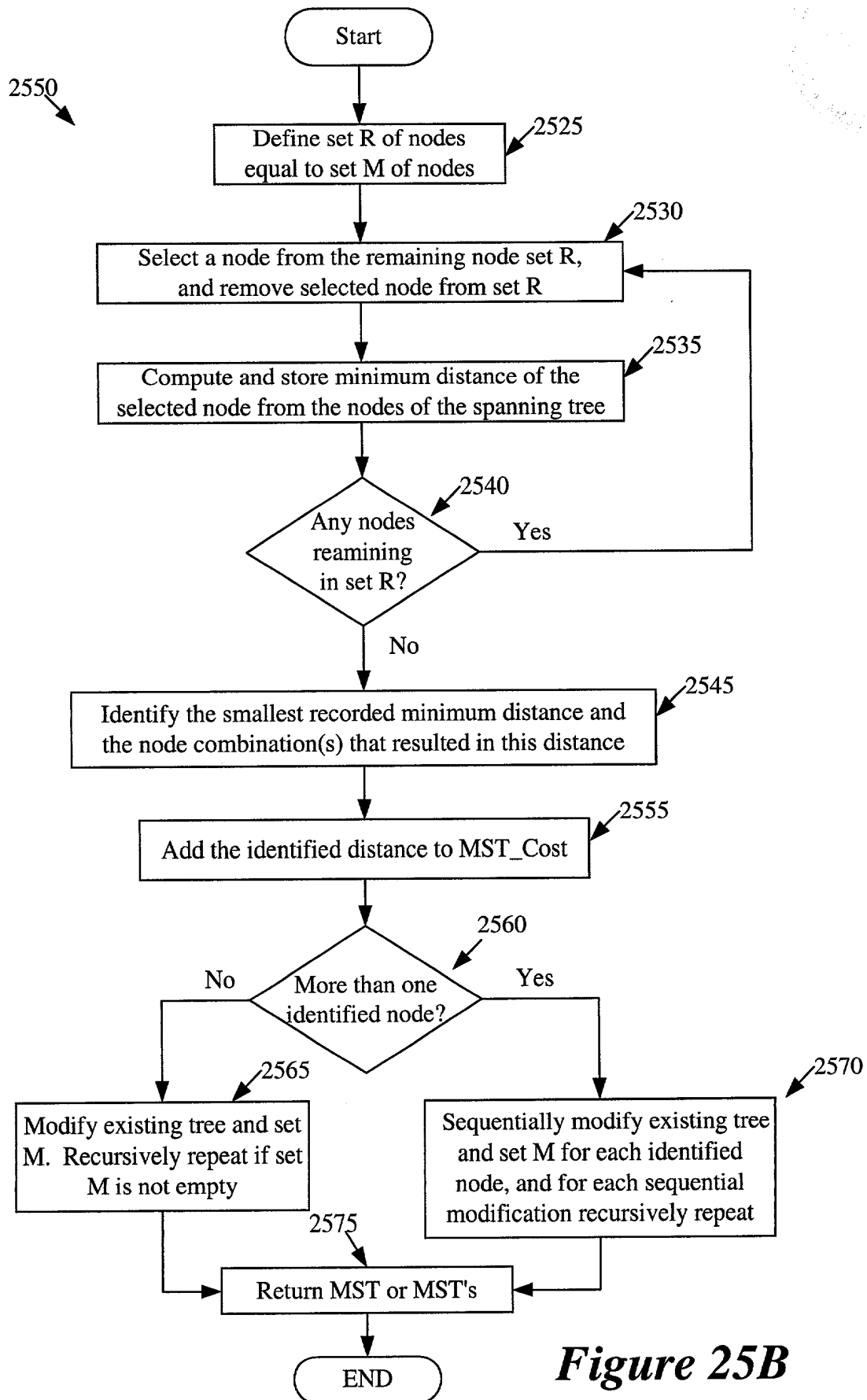


Figure 25B

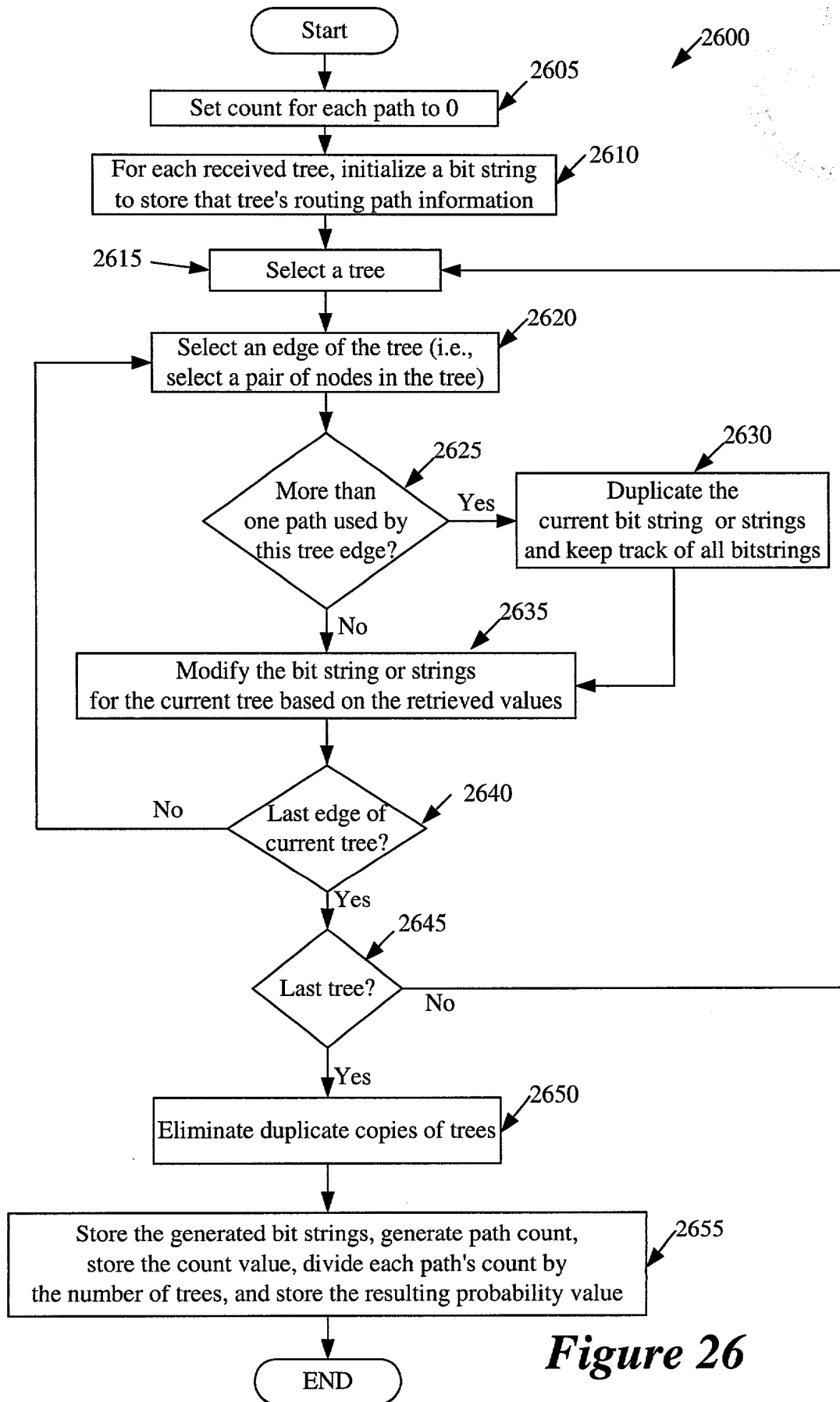


Figure 26

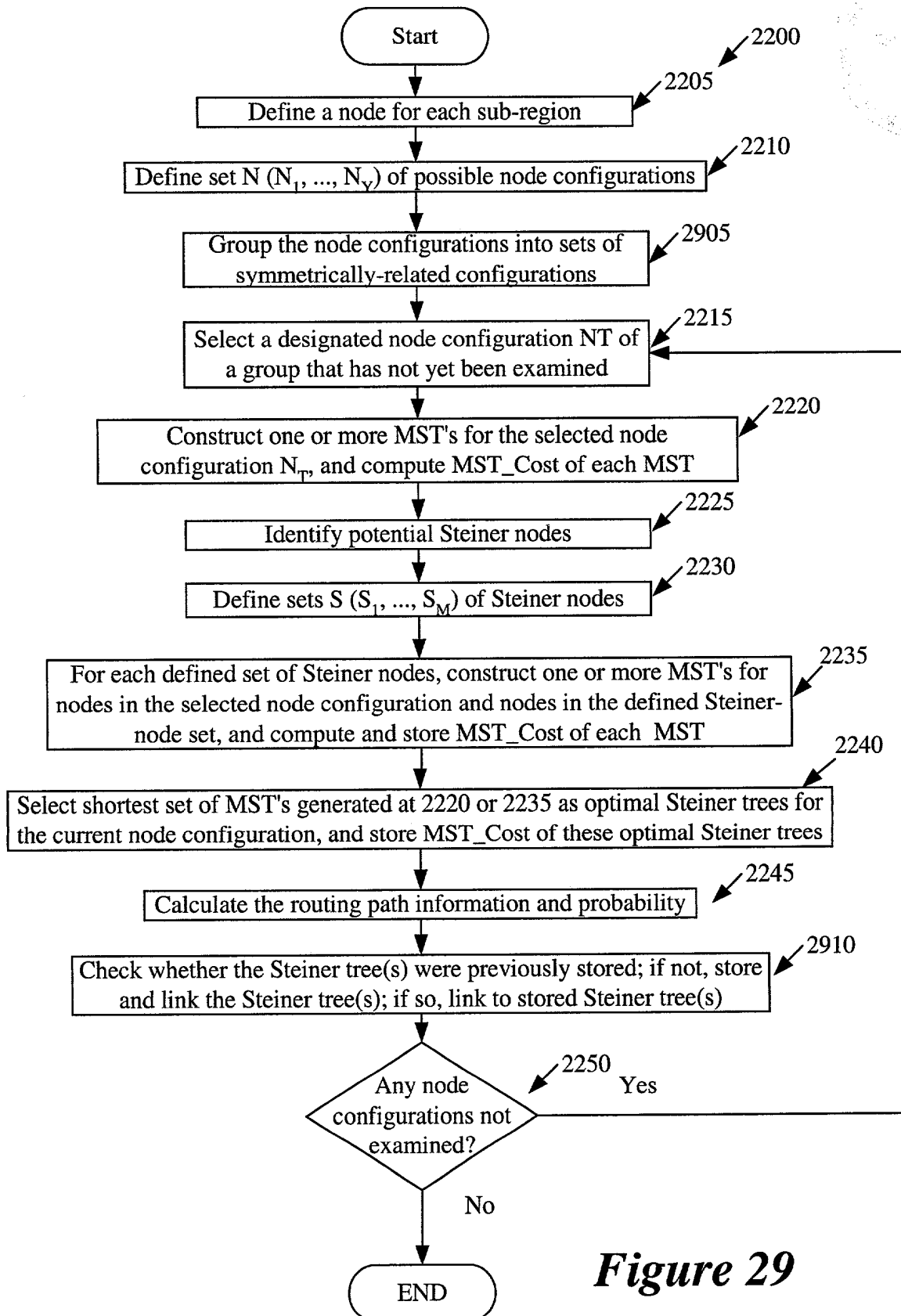


Figure 29

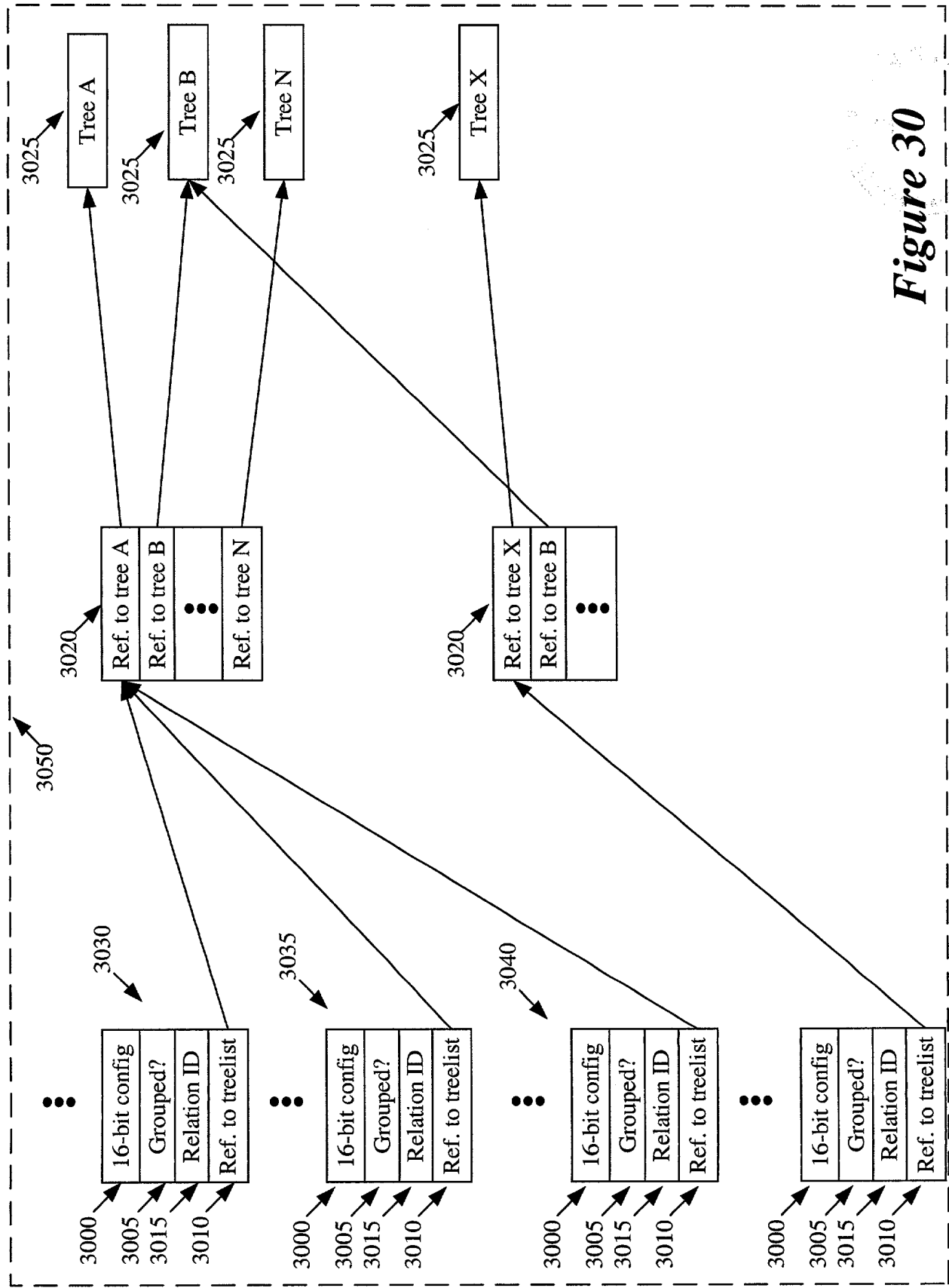


Figure 30

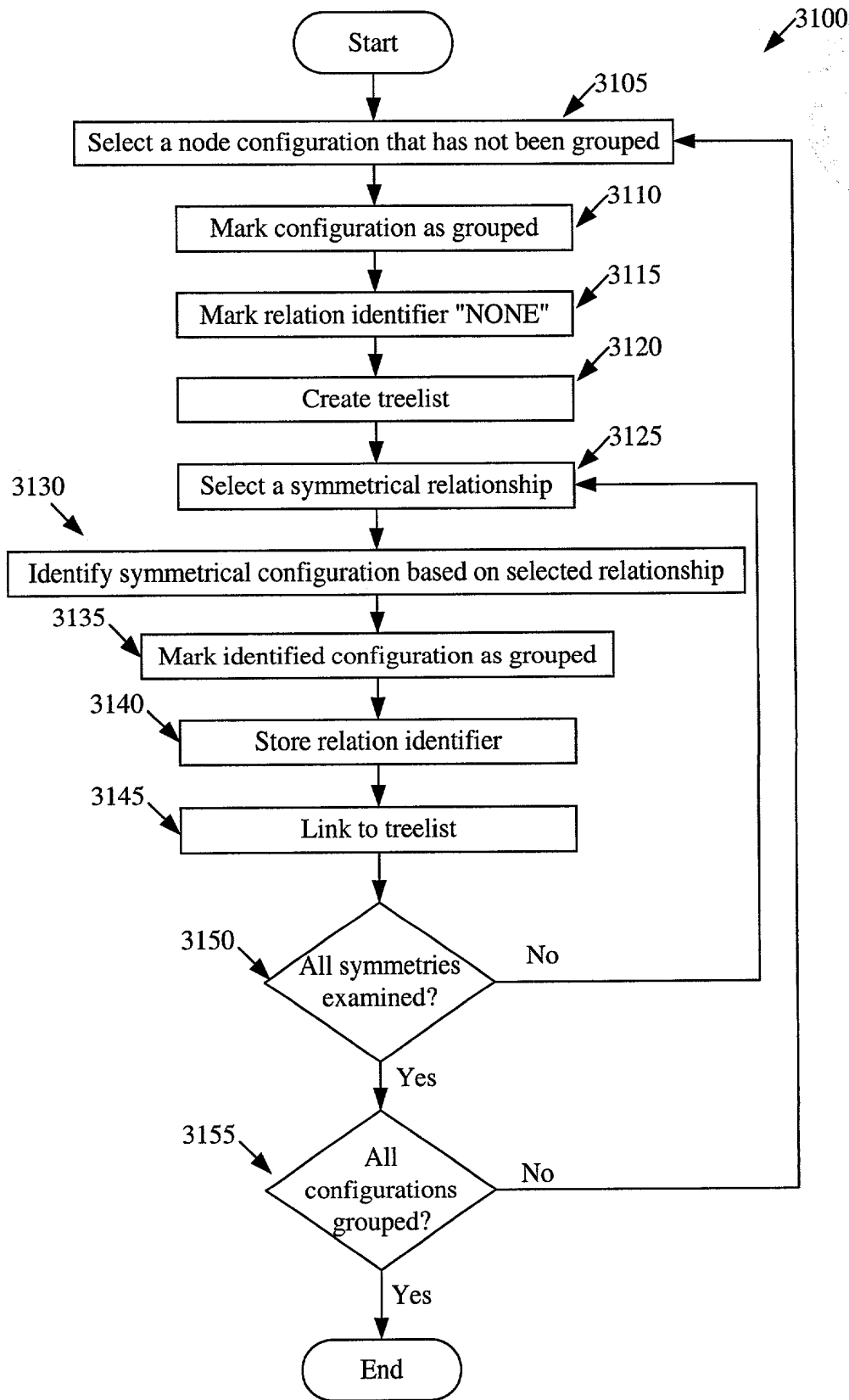


Figure 31

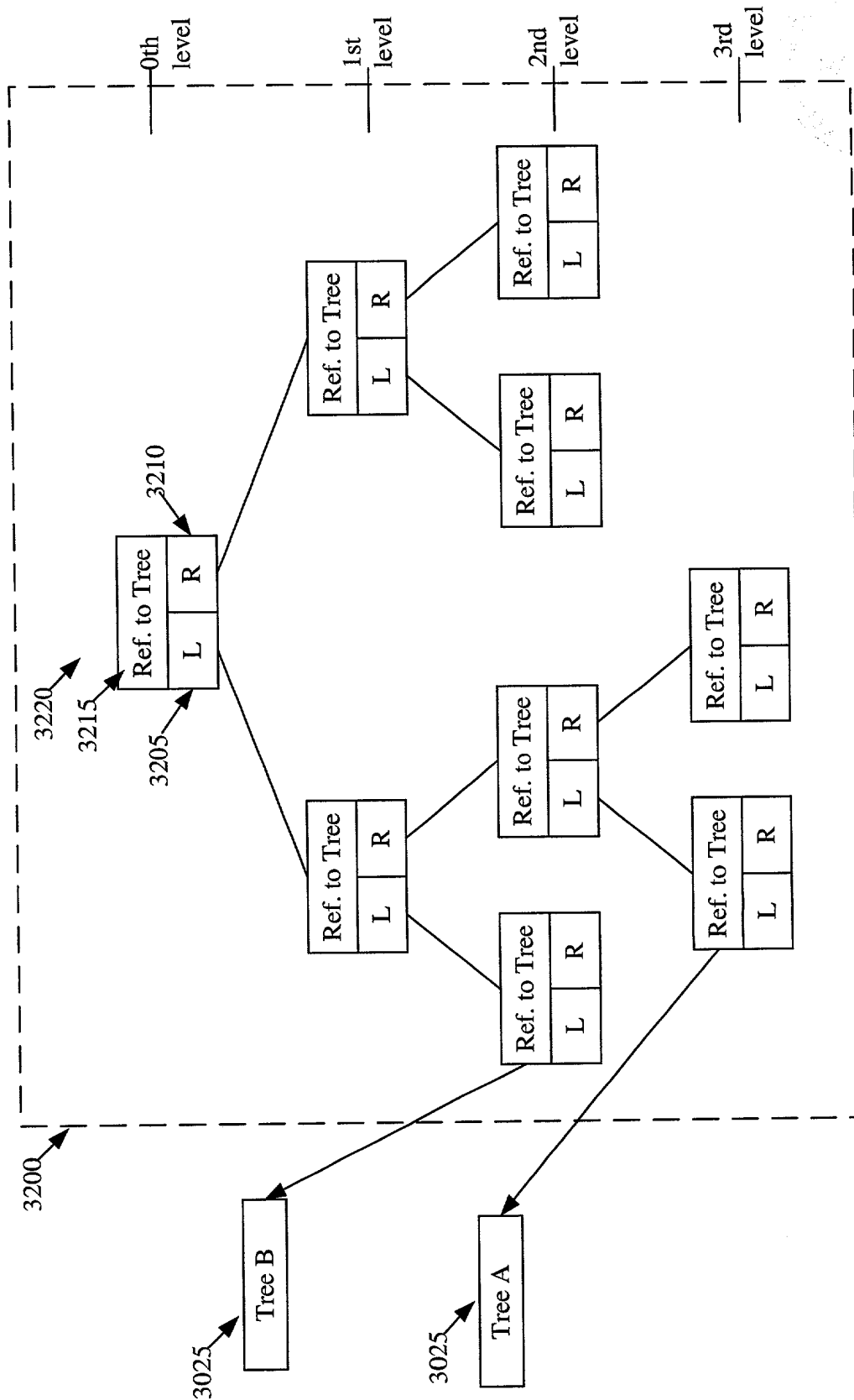


Figure 32

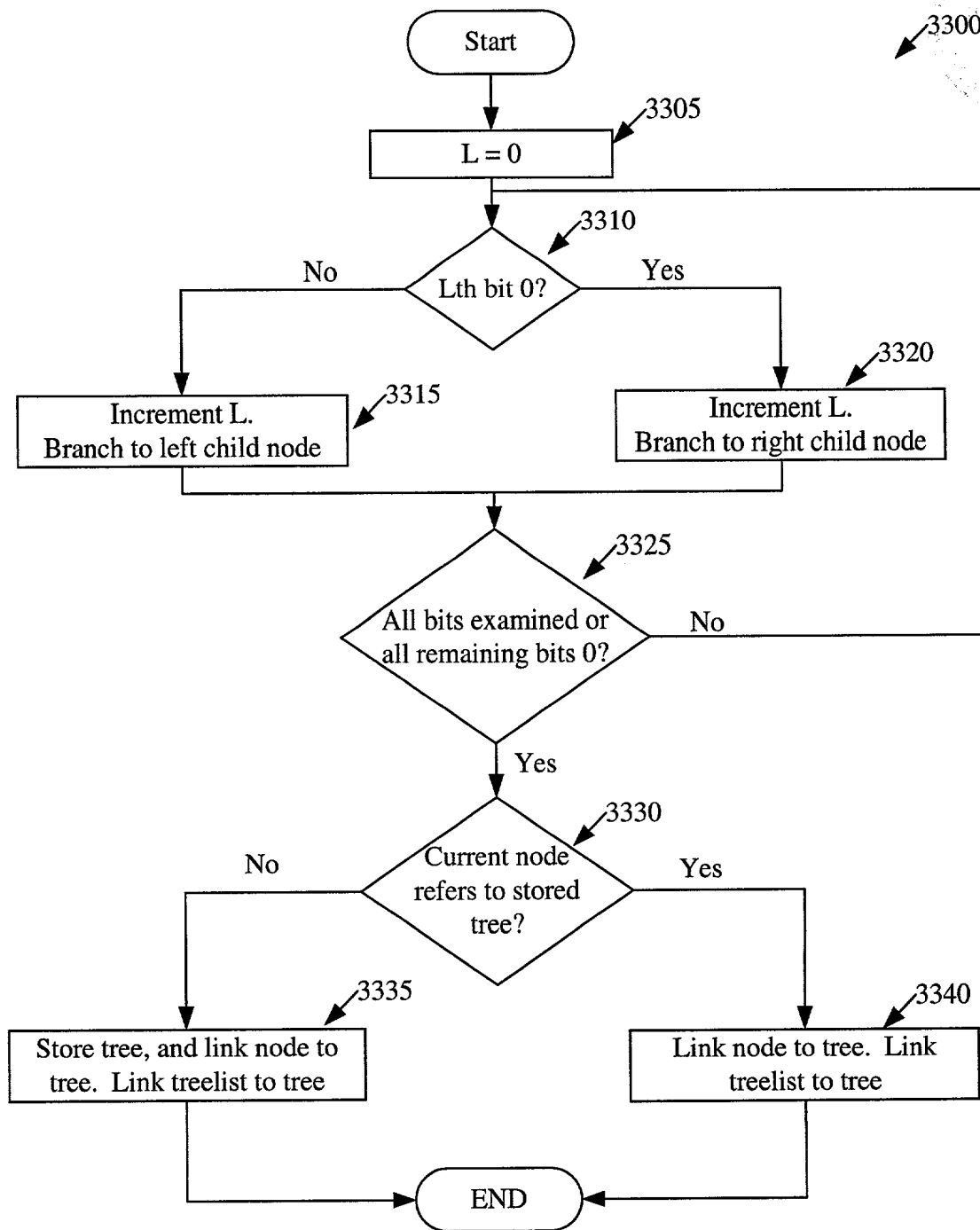


Figure 33

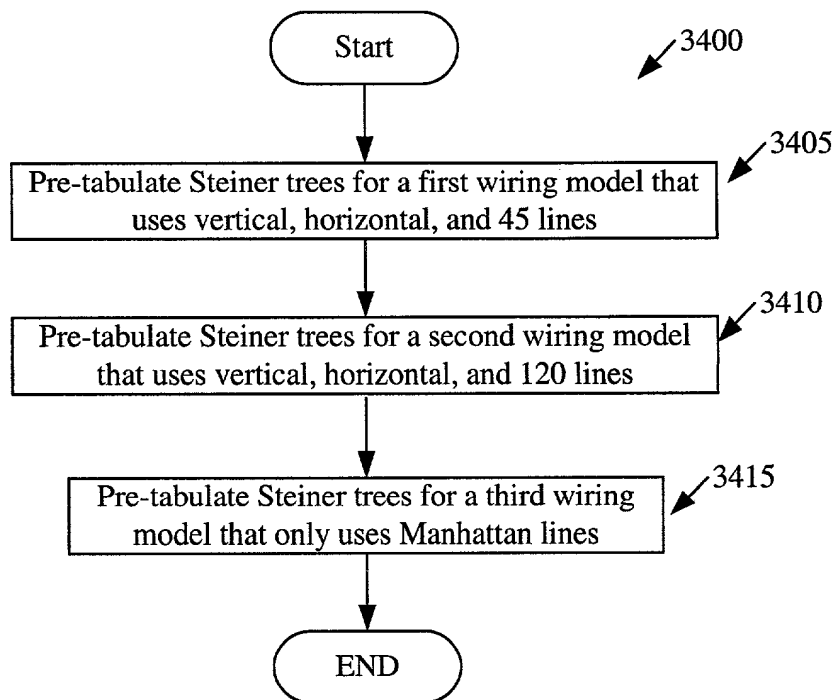


Figure 34

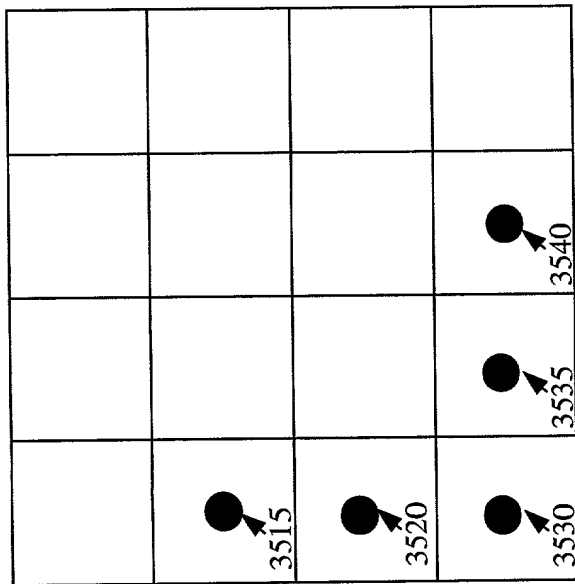


Figure 35A

3505

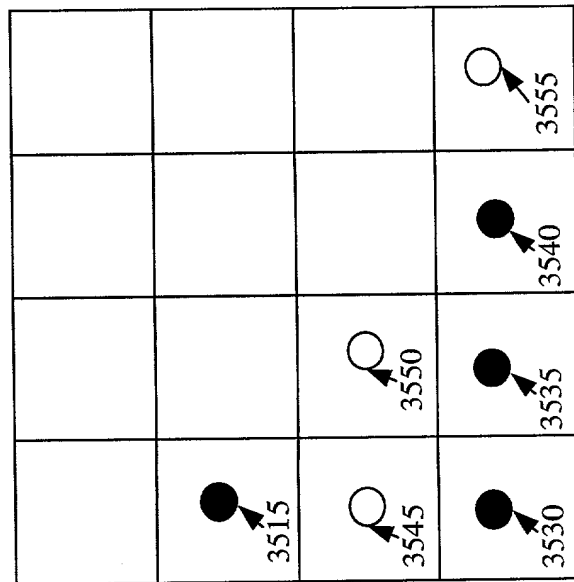
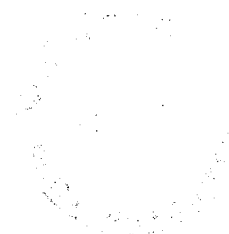


Figure 35B

3510



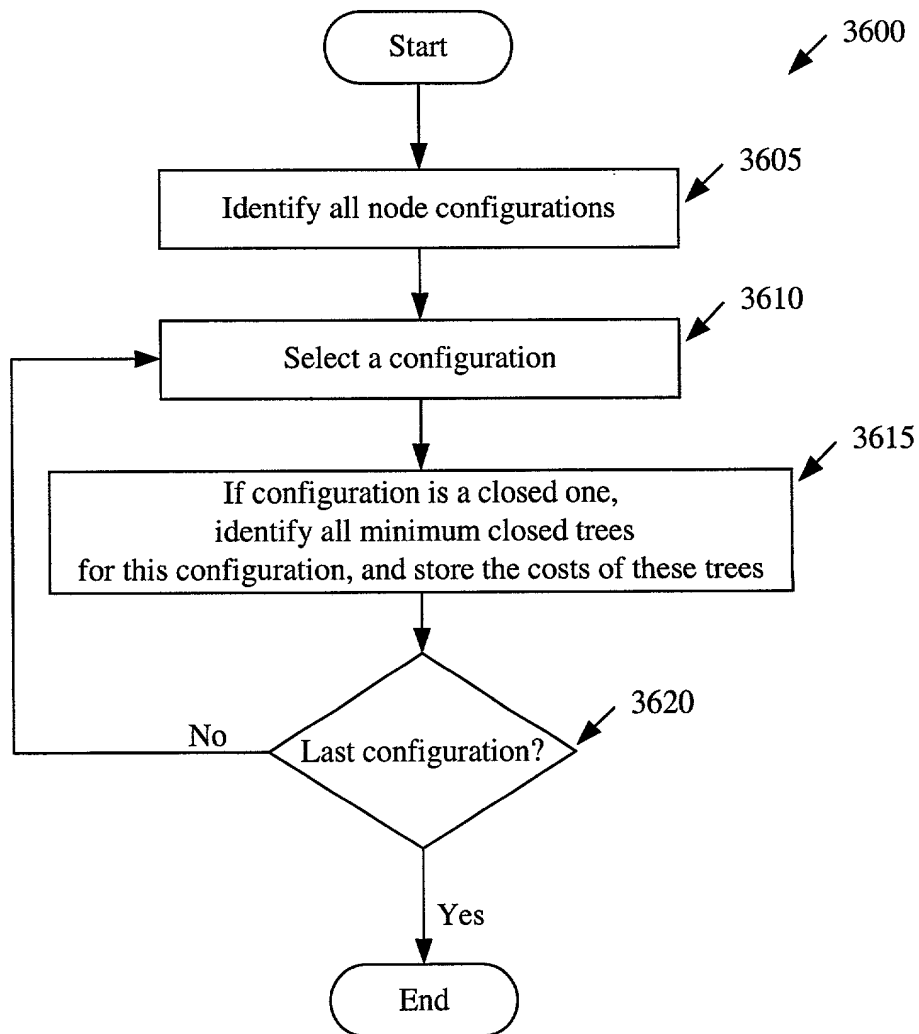


Figure 36

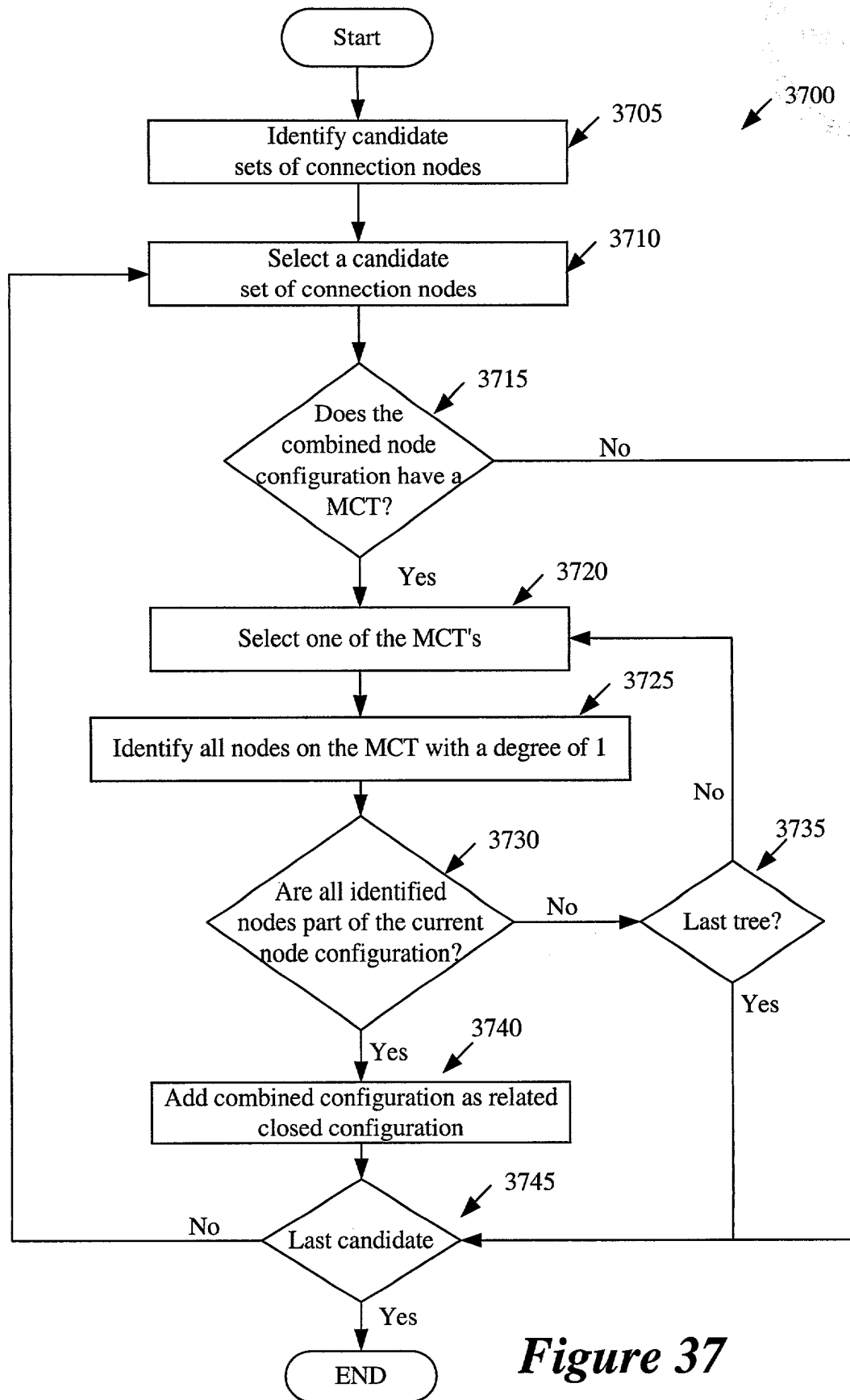


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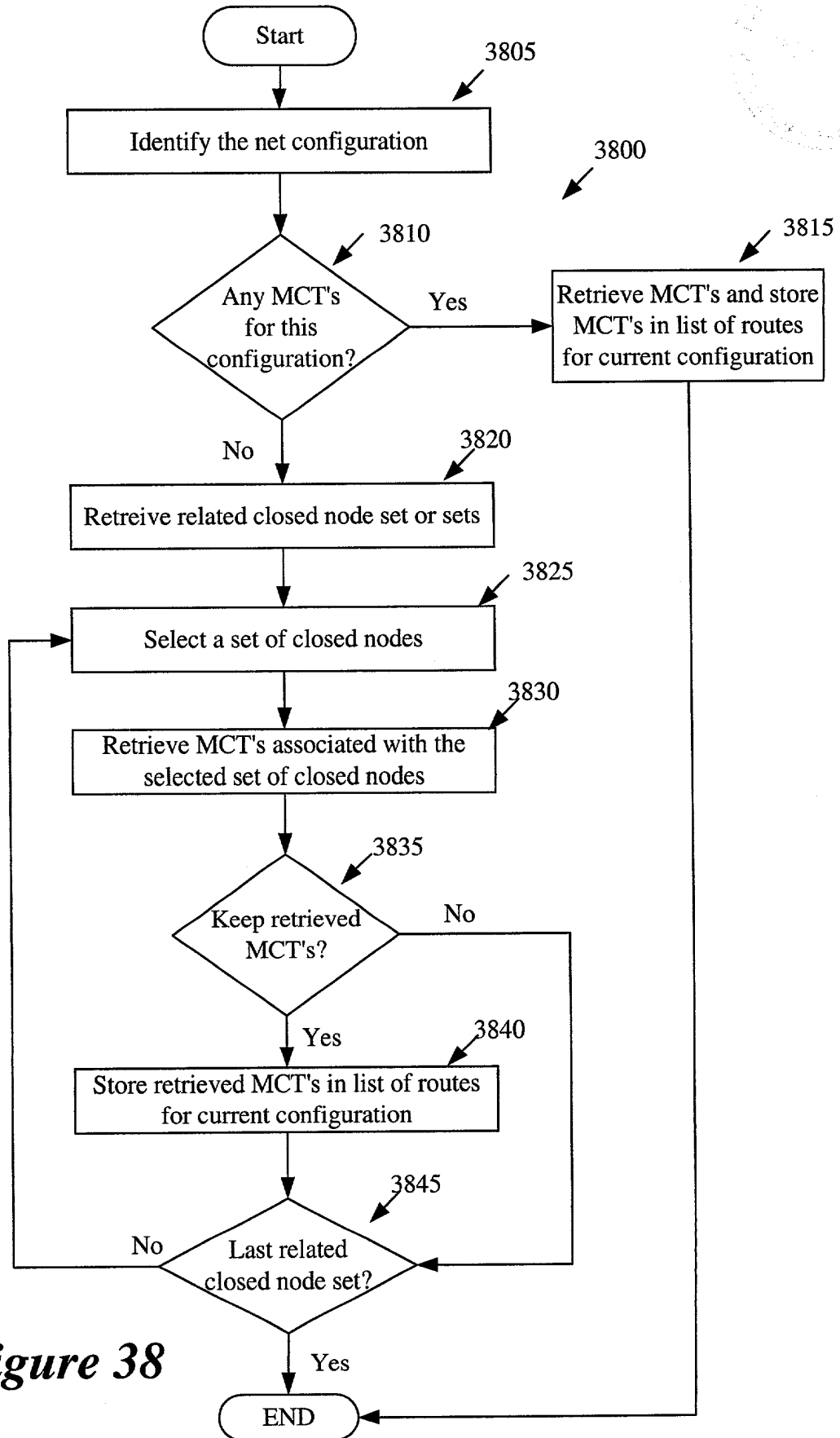


Figure 38

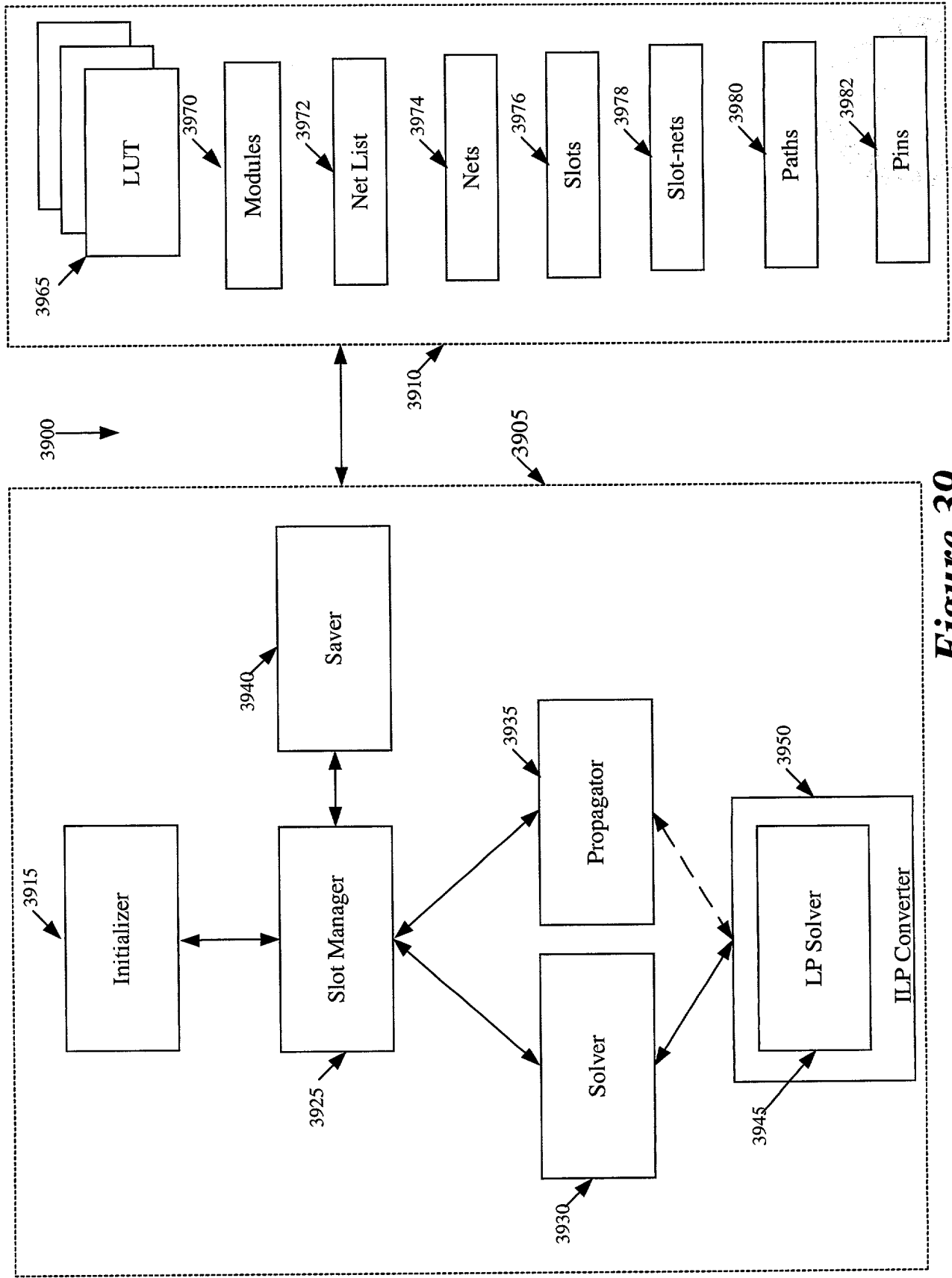


Figure 39

FIG. 40 is a schematic diagram of a grid structure 4000. The grid structure 4000 includes a main grid 4005 and a sub-grid 4010. The main grid 4005 is a large grid of squares, and the sub-grid 4010 is a smaller grid of squares located within the main grid 4005. The sub-grid 4010 is located in the bottom-left corner of the main grid 4005.

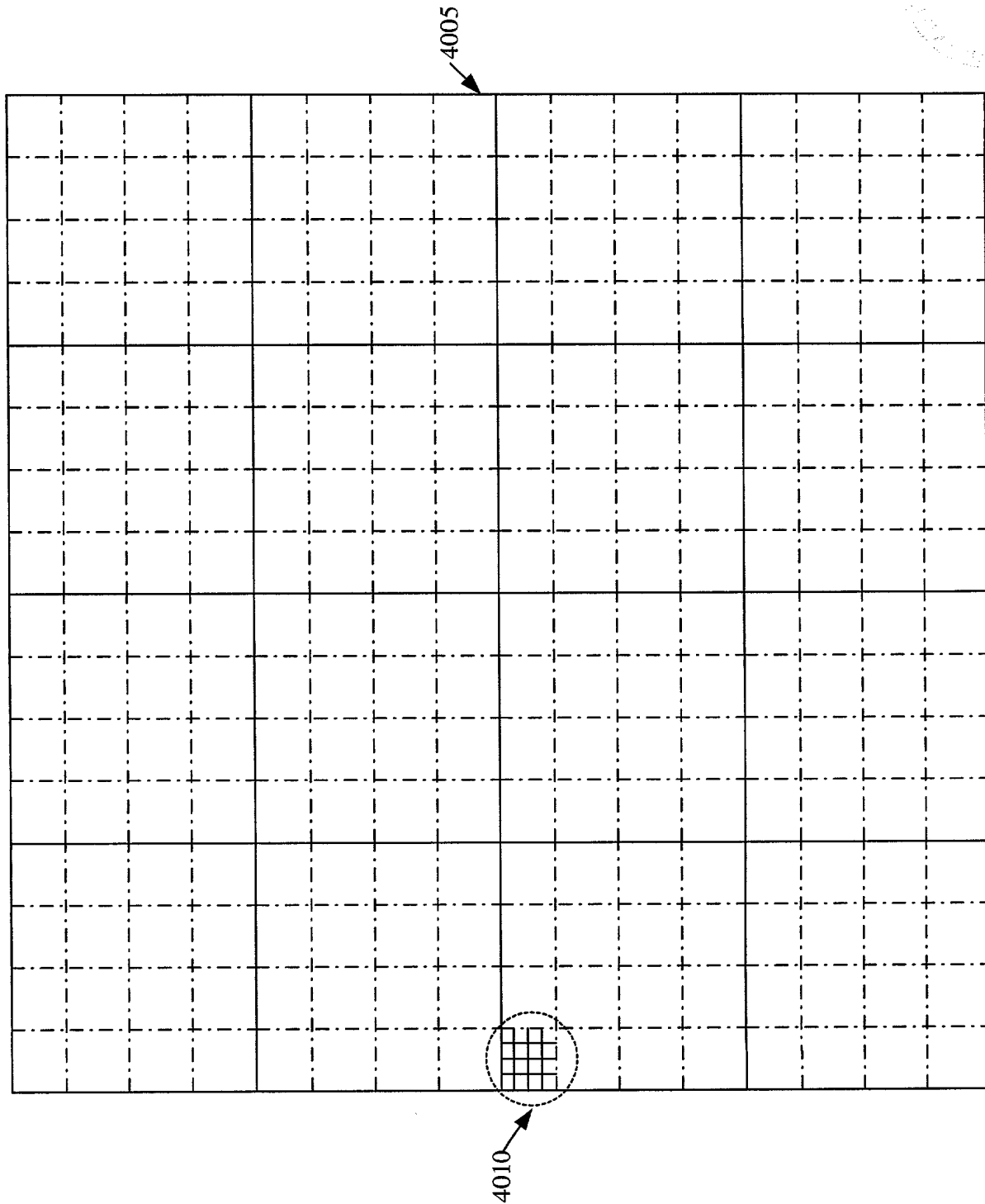


Figure 40

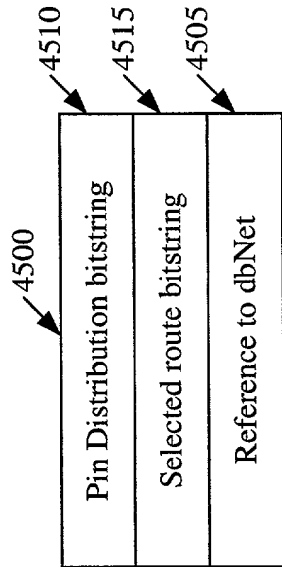


Figure 45

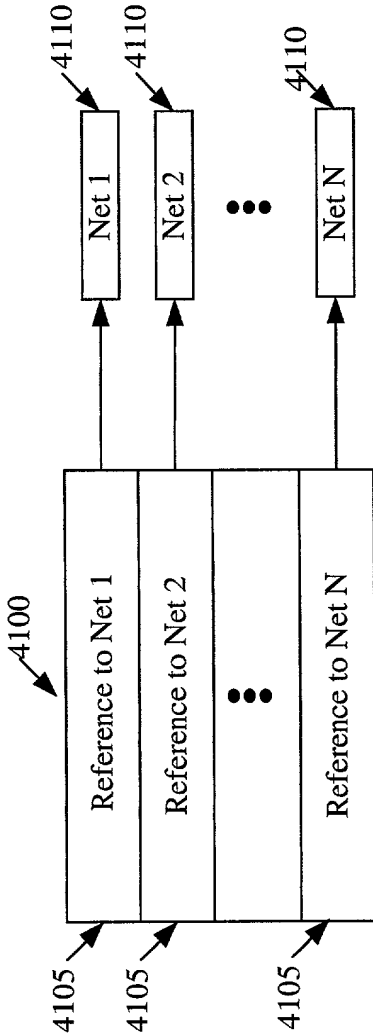


Figure 41

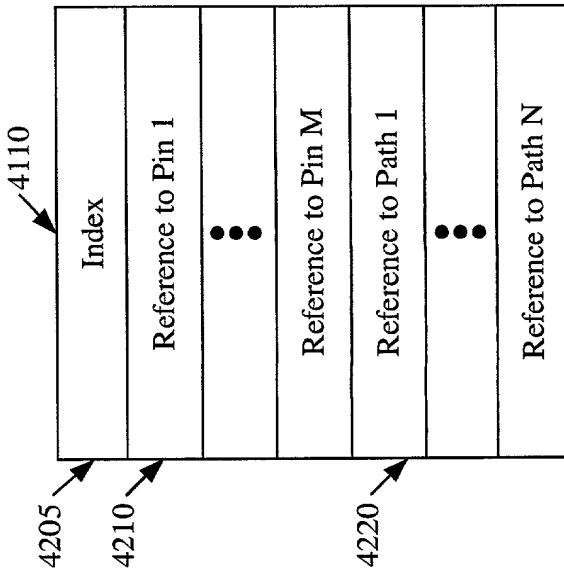


Figure 42

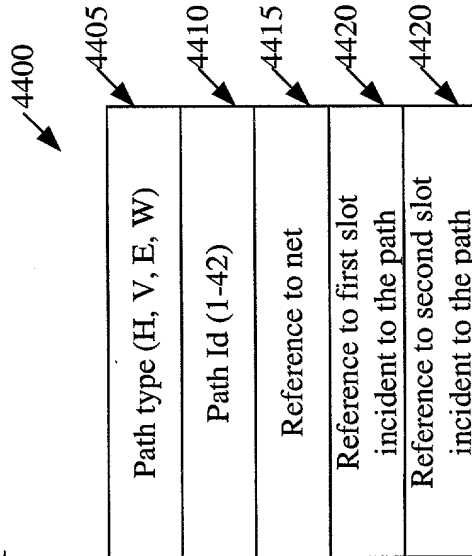


Figure 44

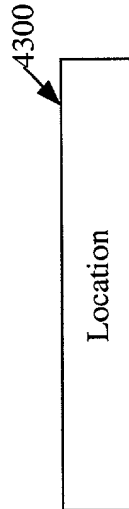


Figure 43

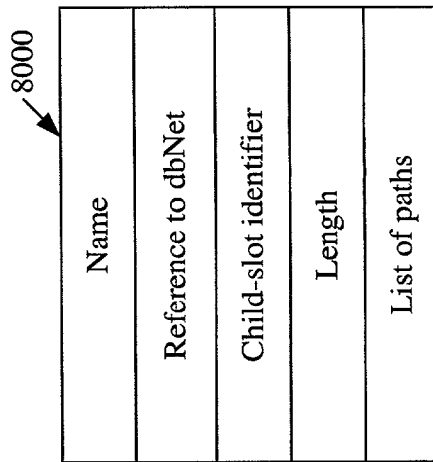


Figure 80

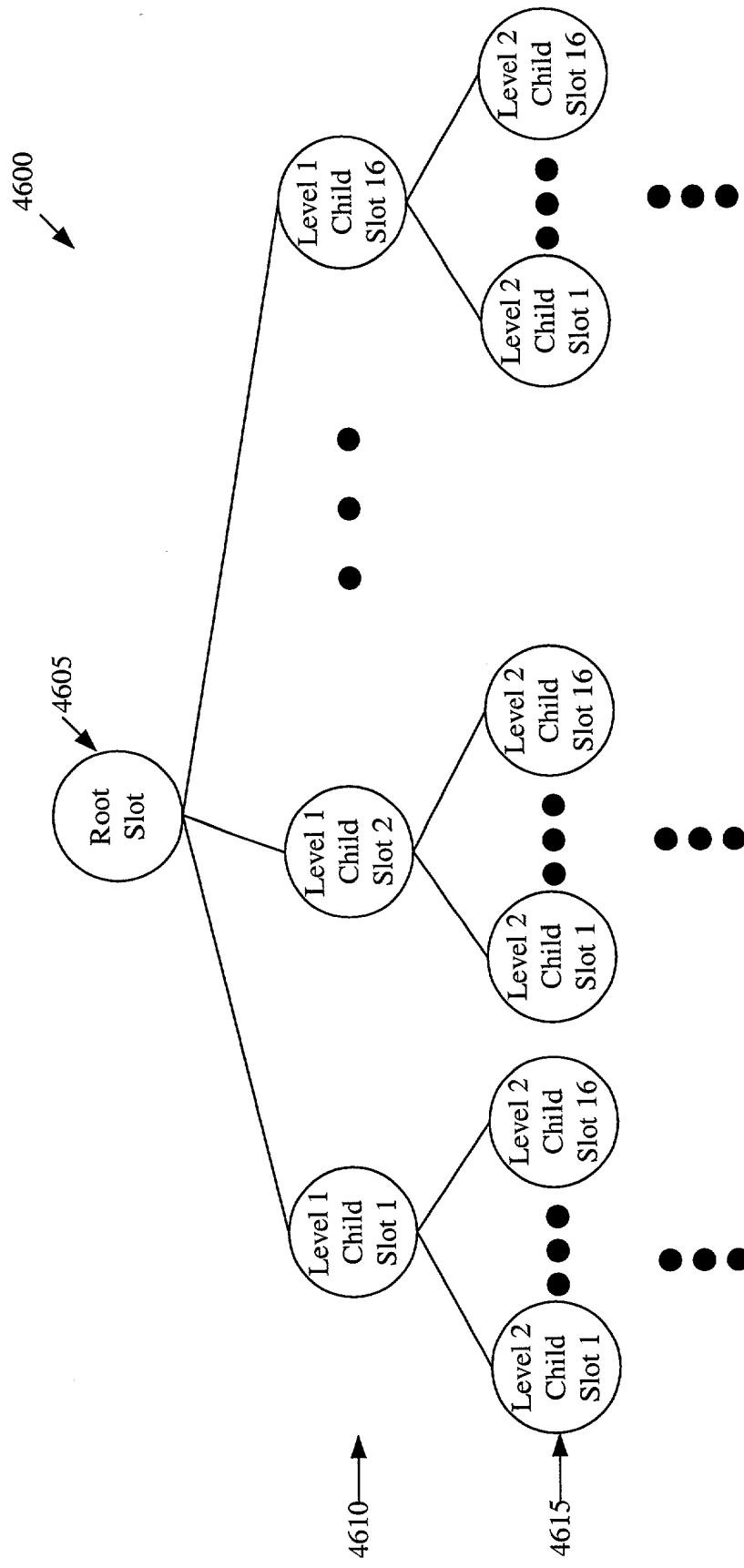


Figure 46

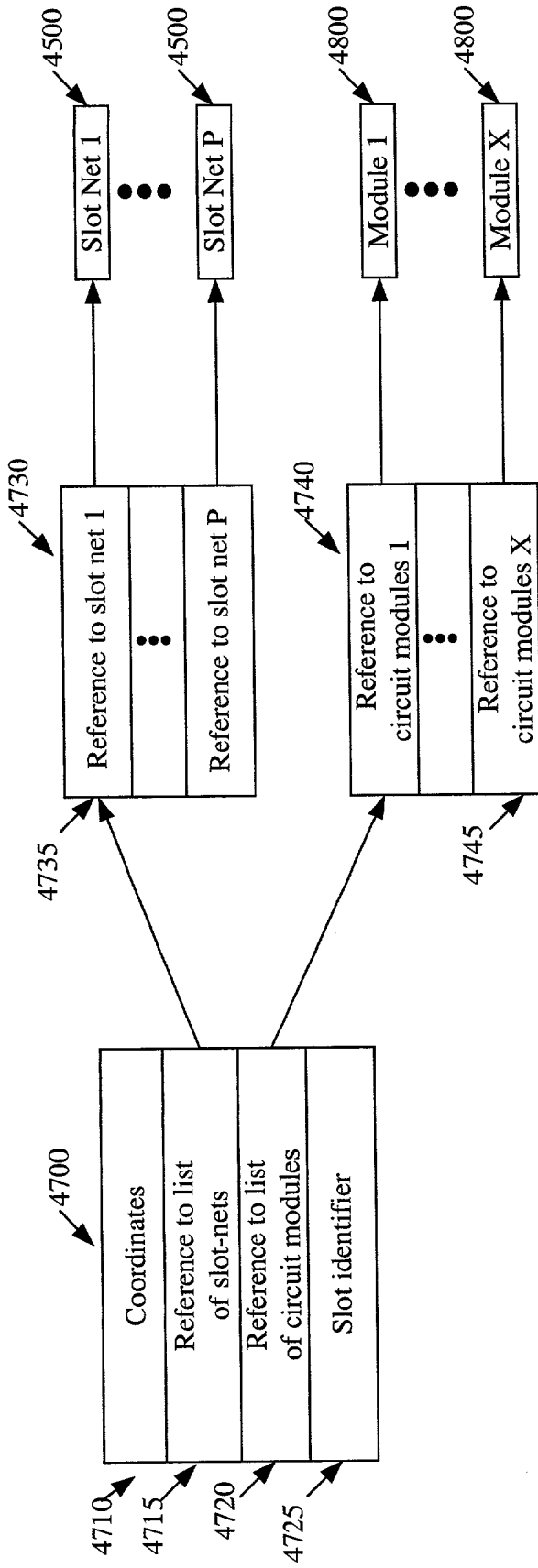


Figure 47

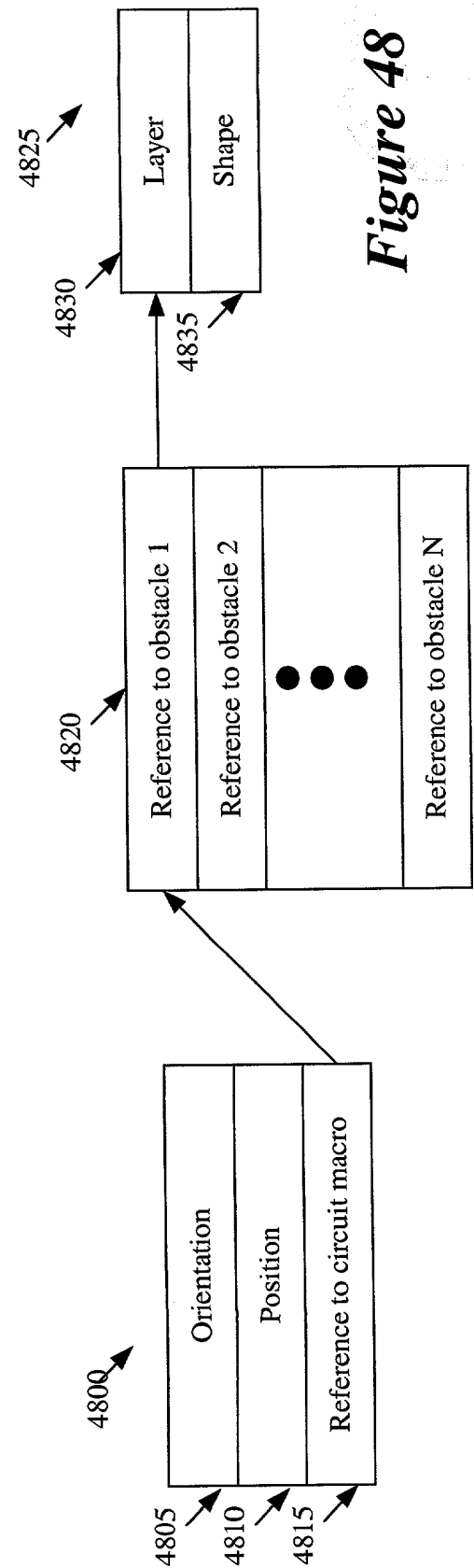


Figure 48

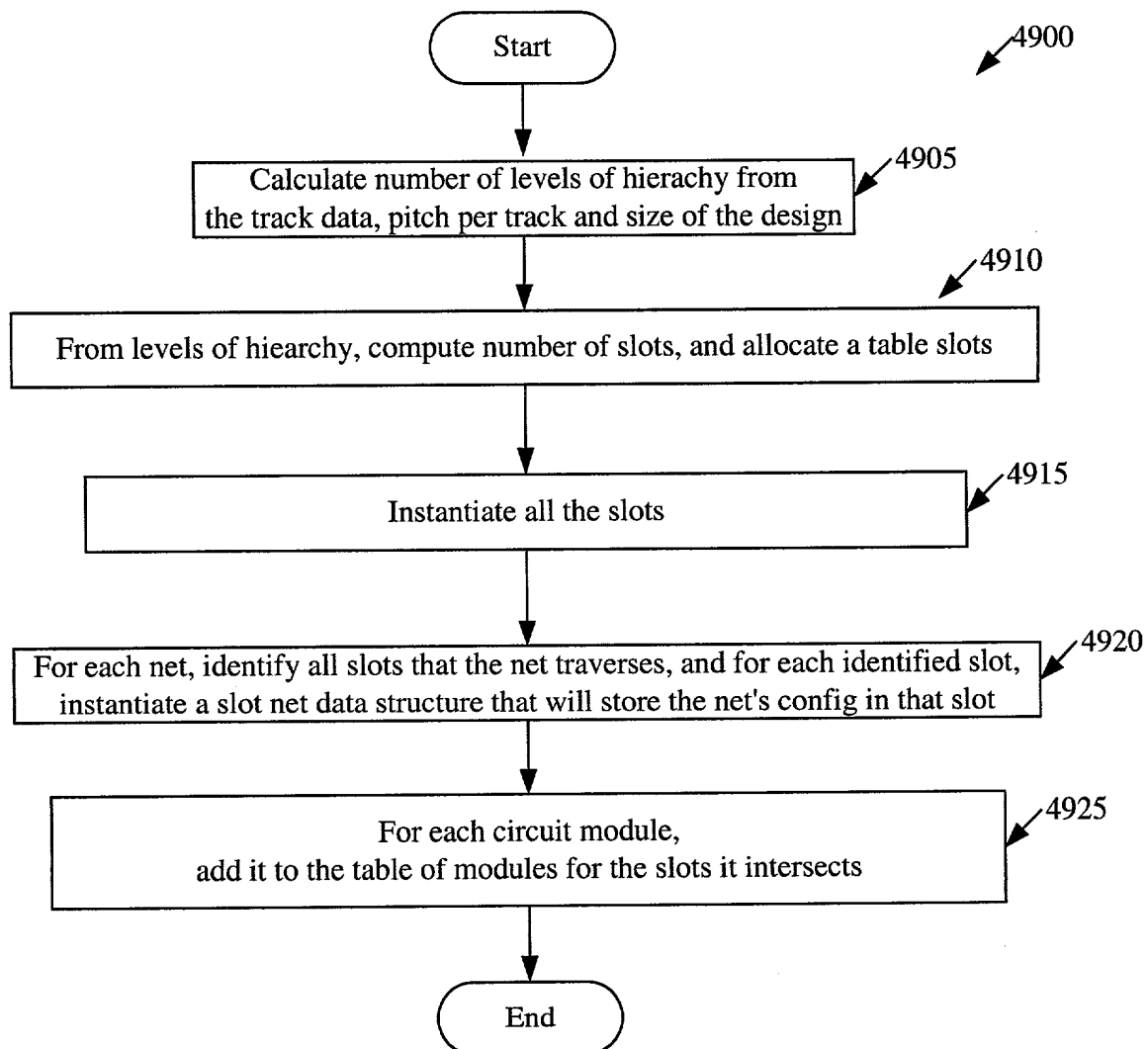


Figure 49

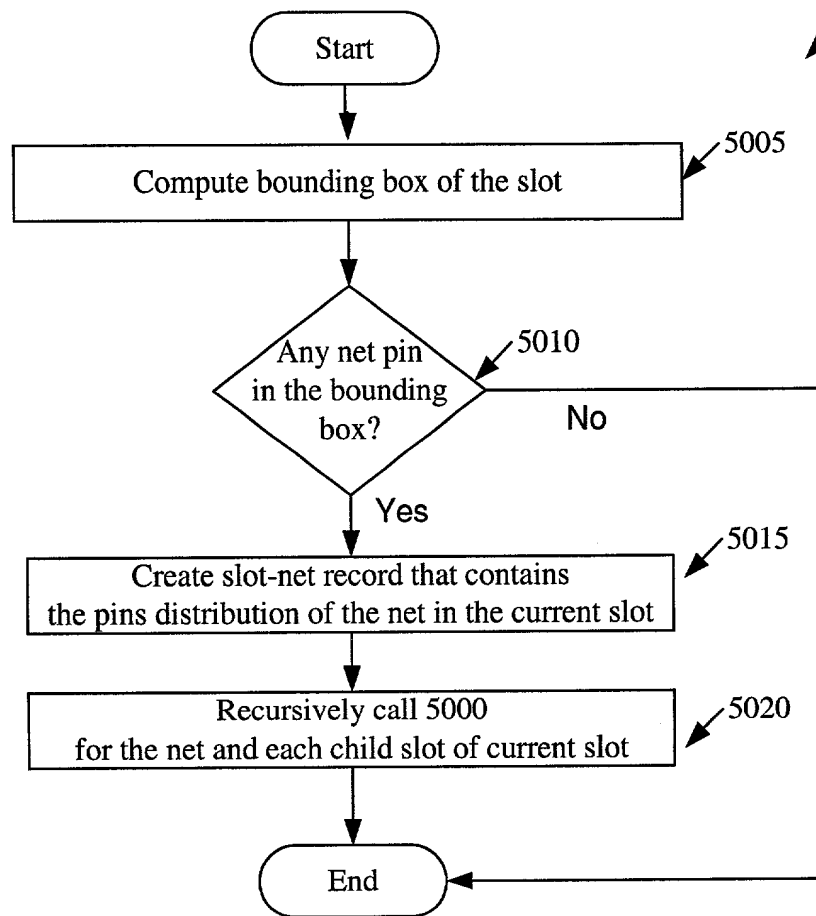


Figure 50

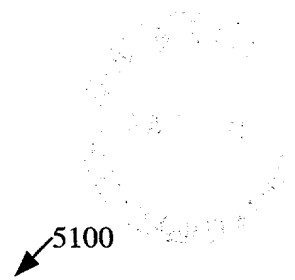
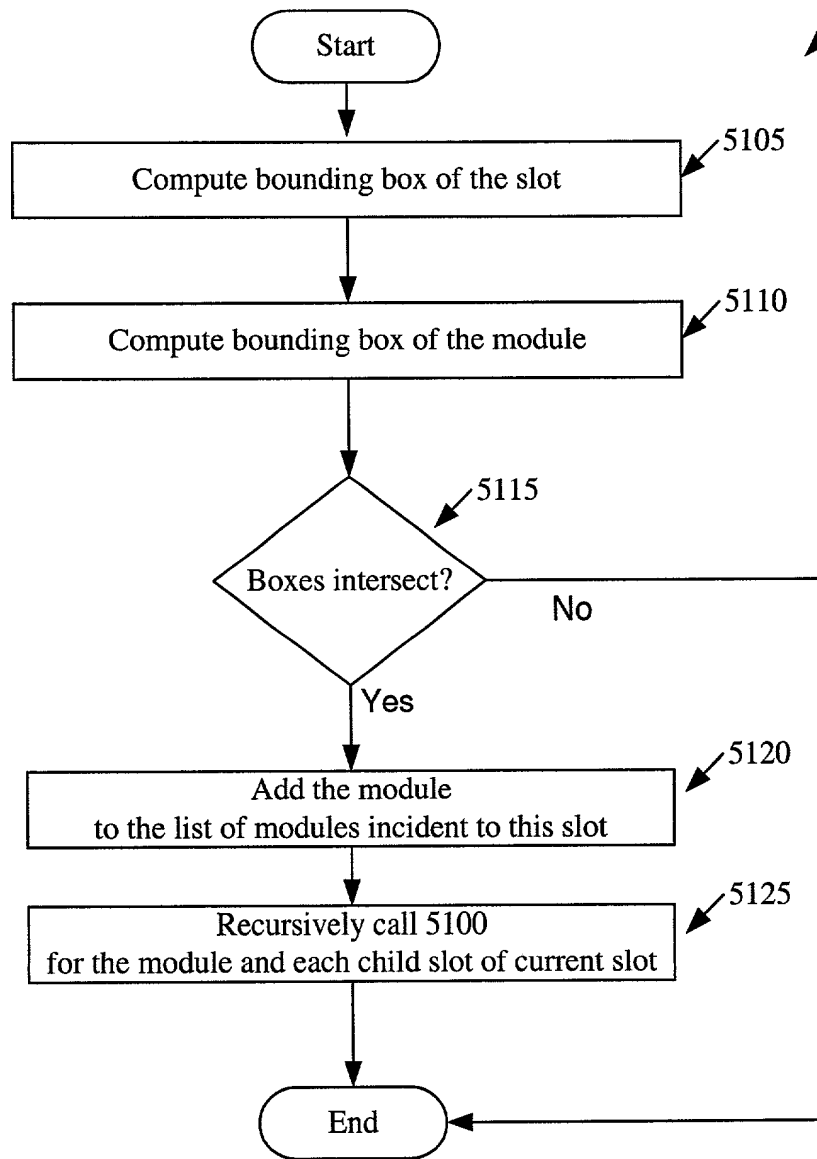


Figure 51

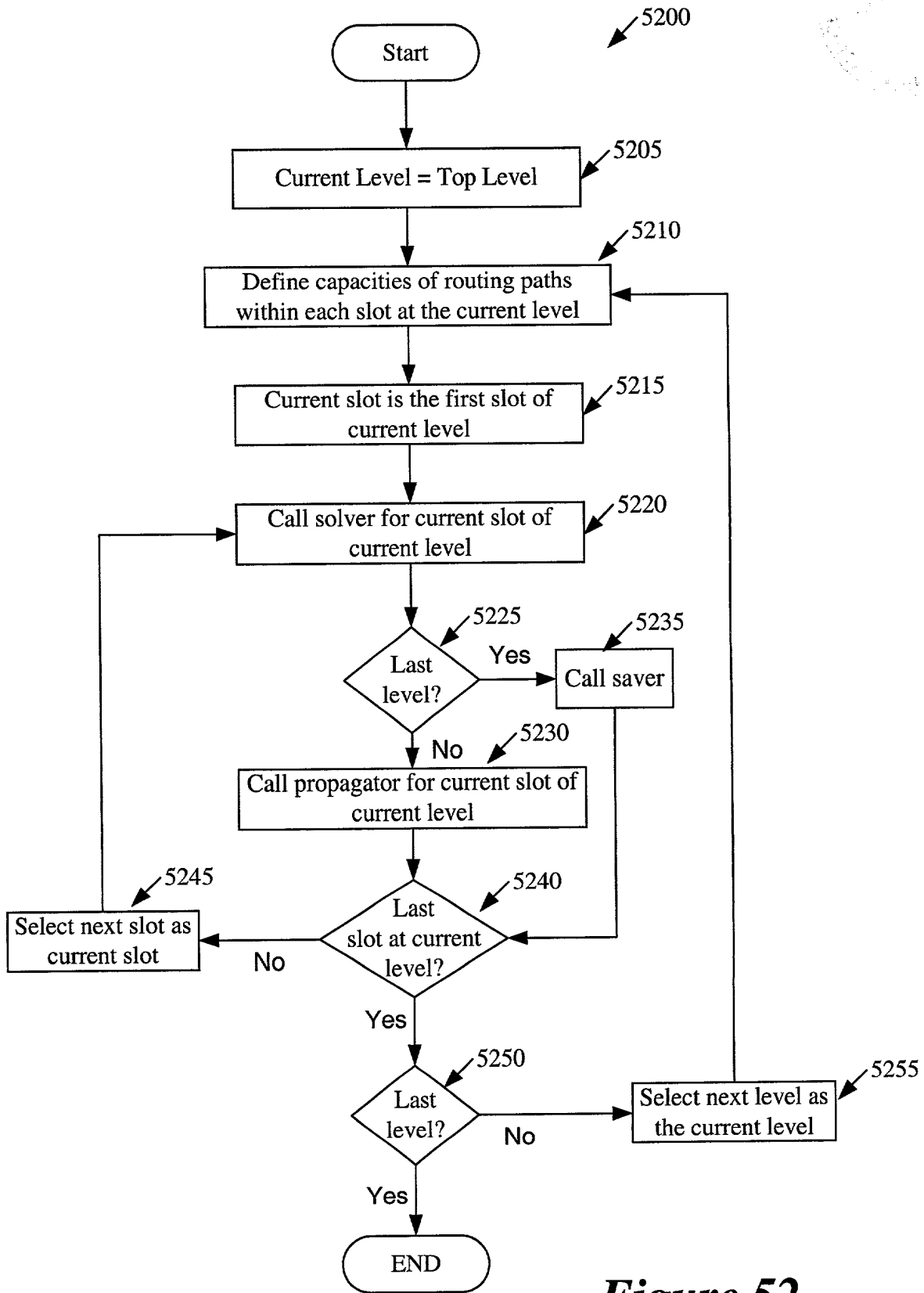


Figure 52

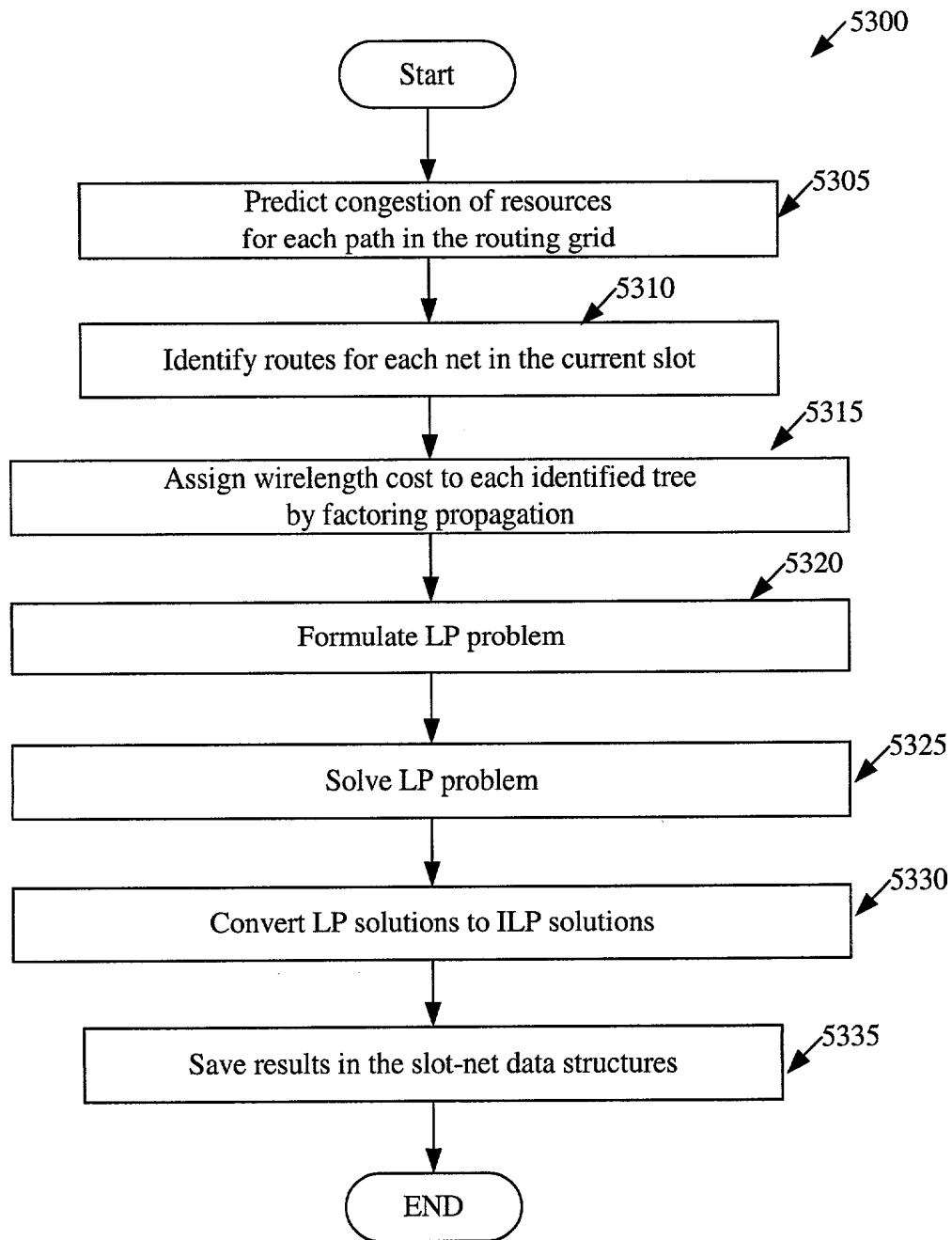


Figure 53

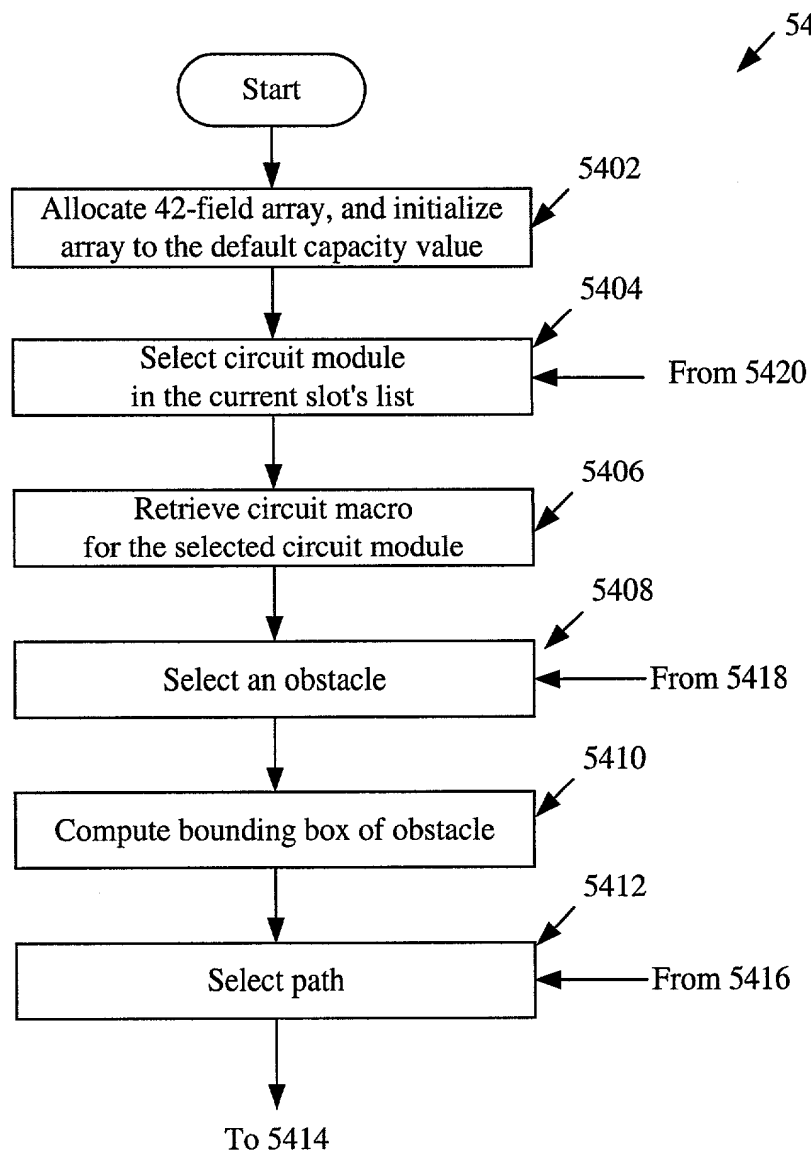


Figure 54A

Figure 54: Figure 54A
Figure 54B

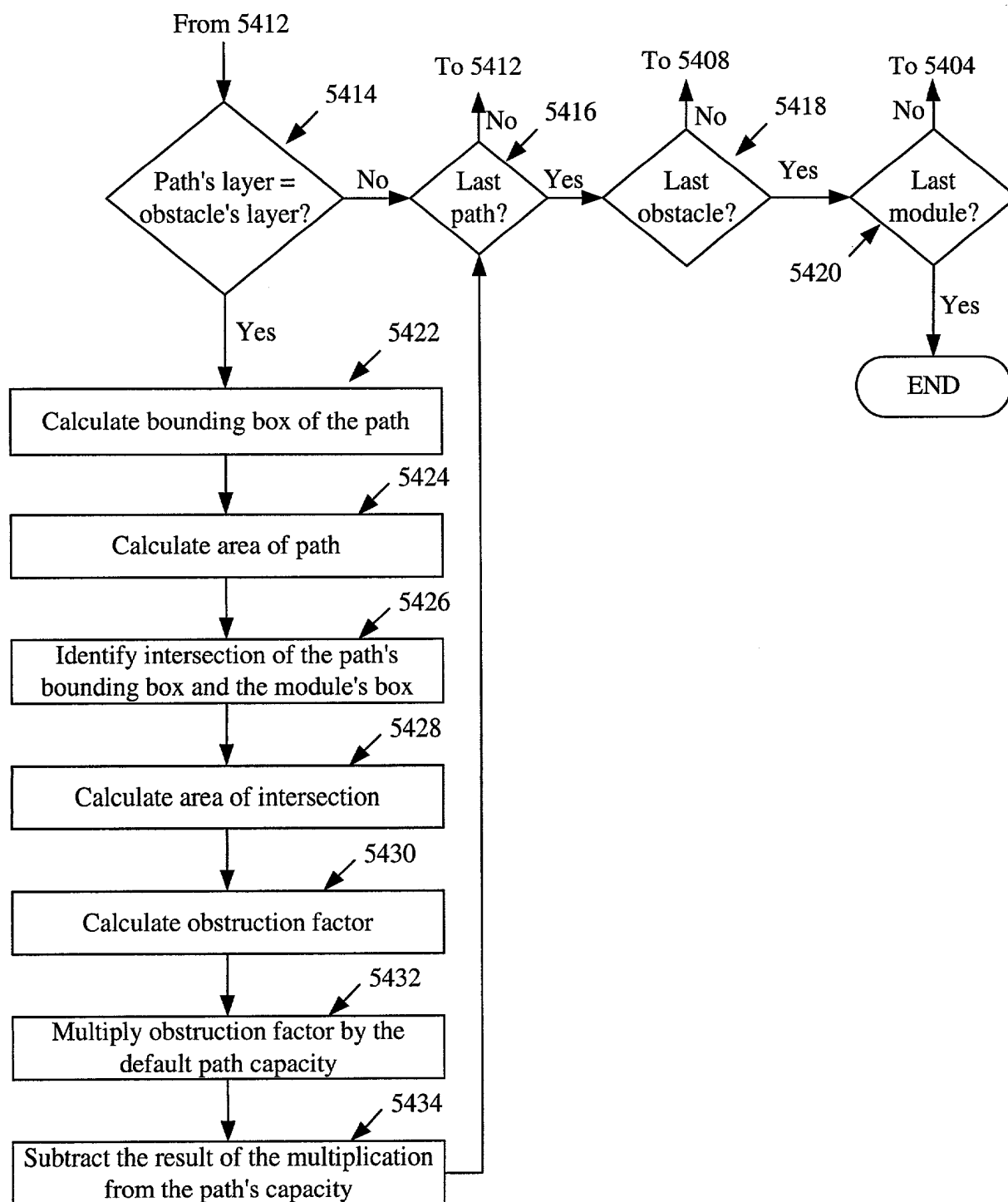


Figure 54B

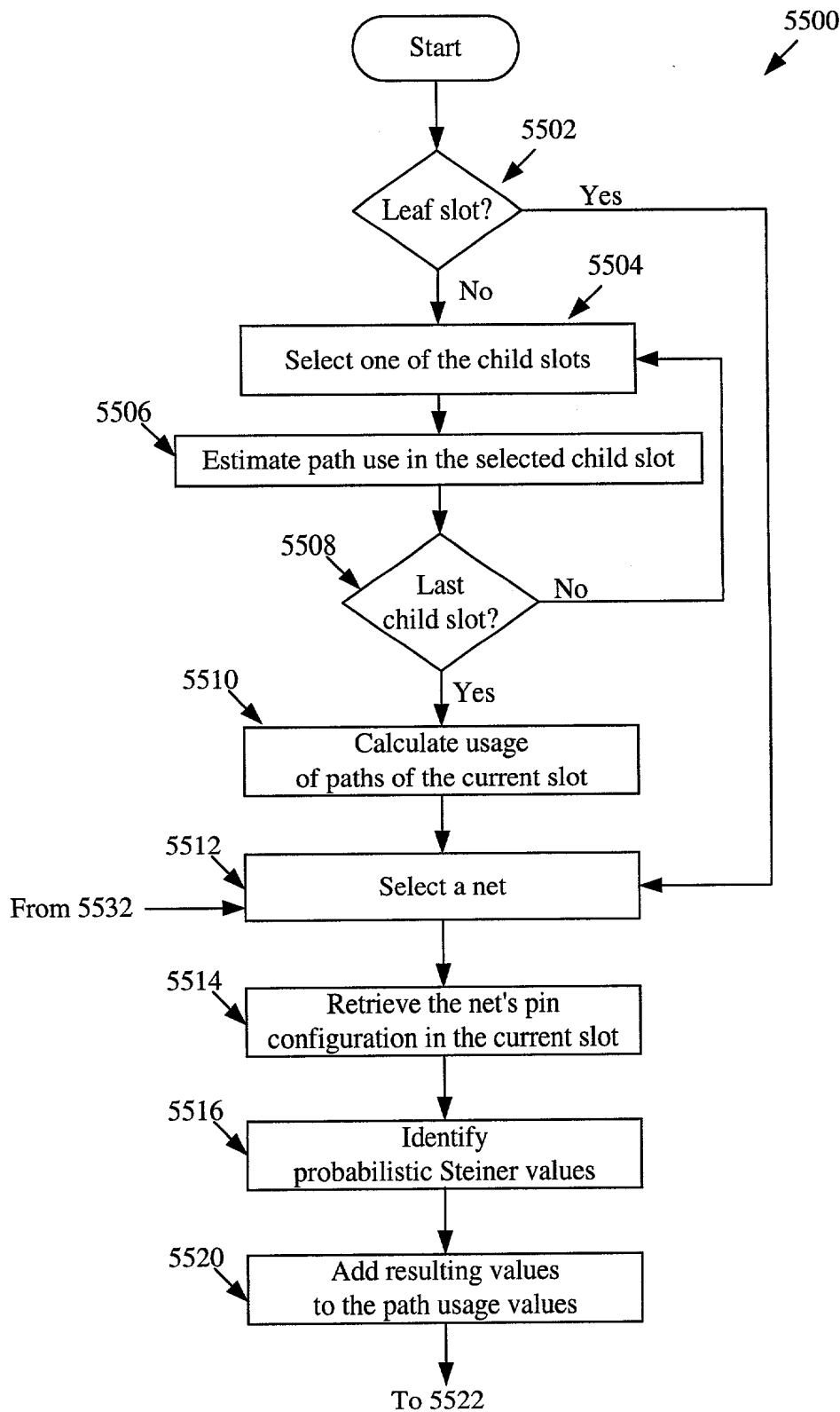


Figure 55A

Figure 55: Figure 55B

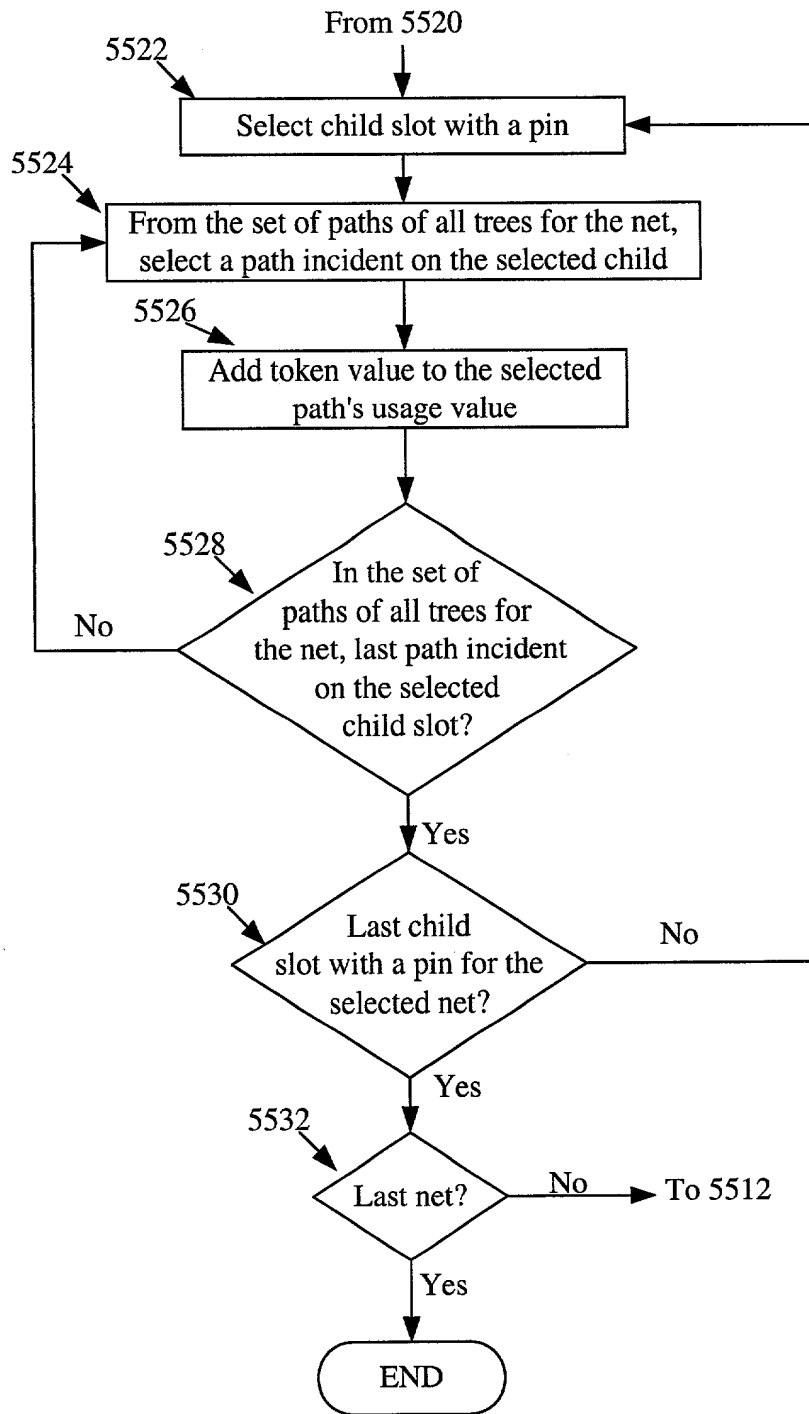


Figure 55B

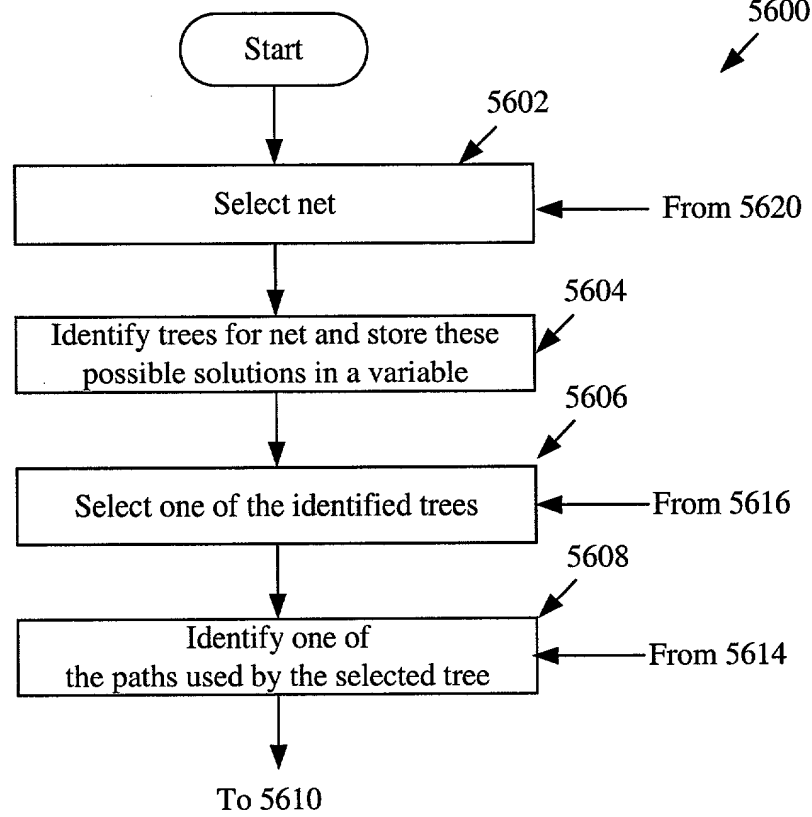


Figure 56A

Figure 56: Figure 56A
Figure 56B
Figure 56C
Figure 56D

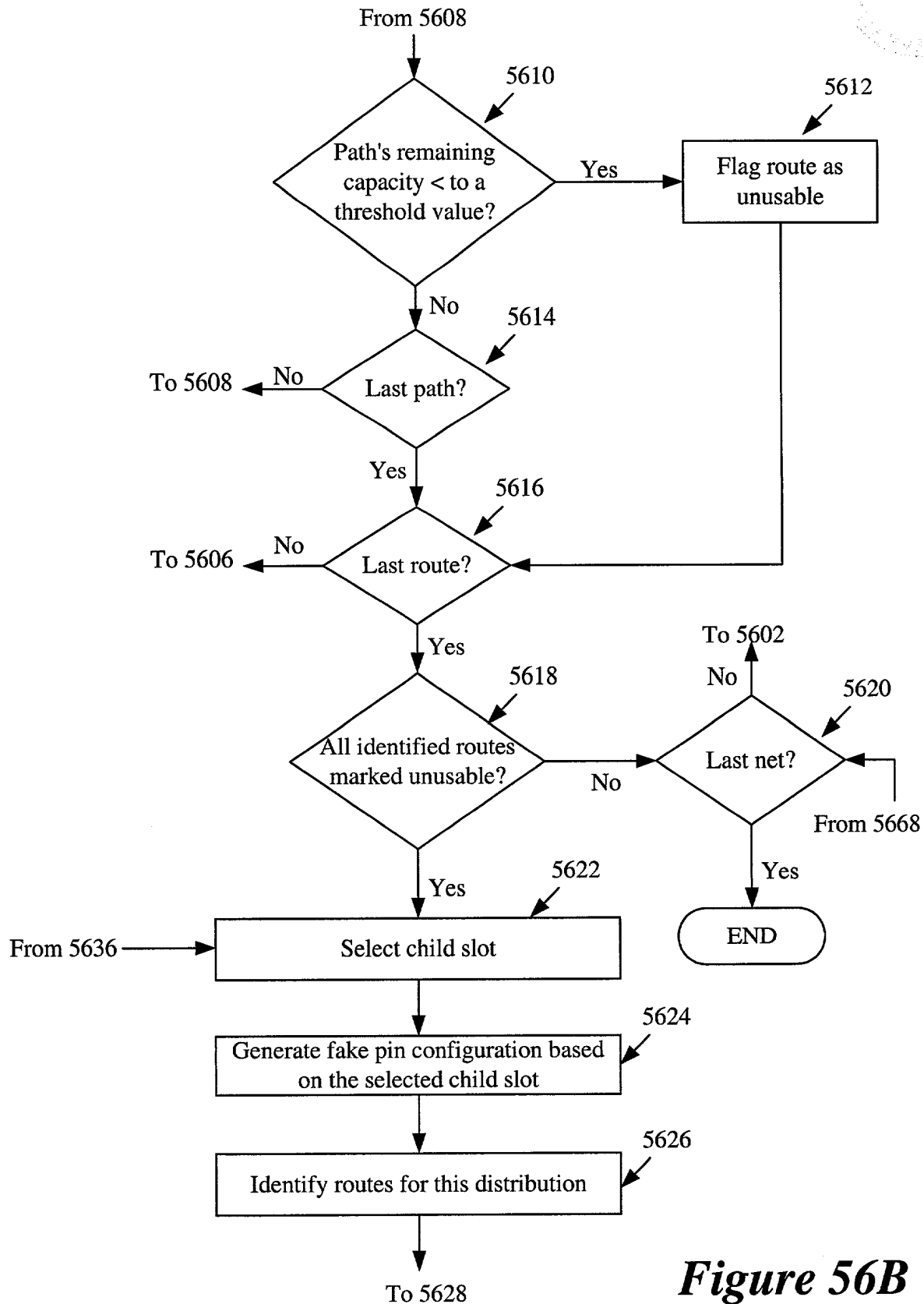


Figure 56B

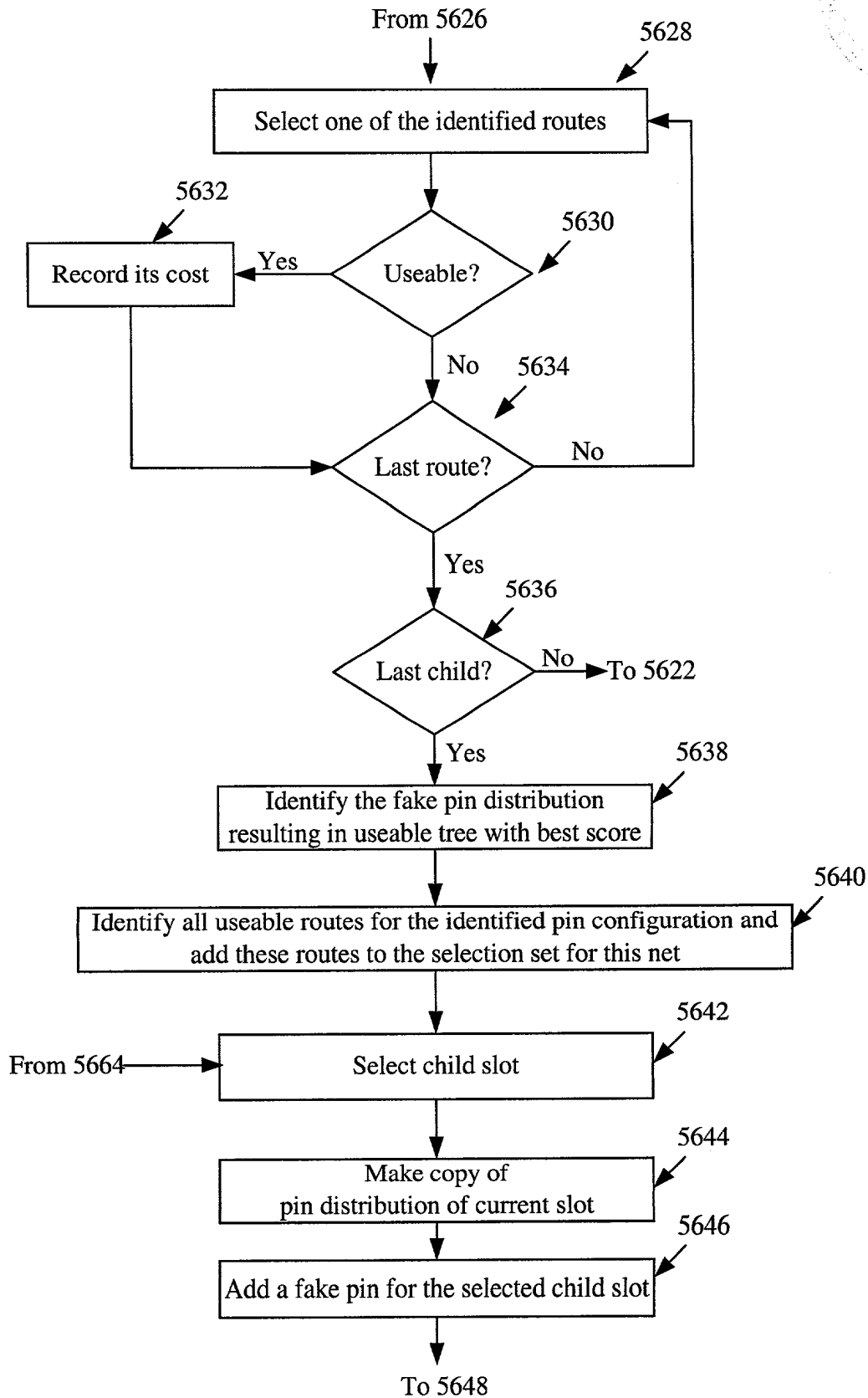


Figure 56C

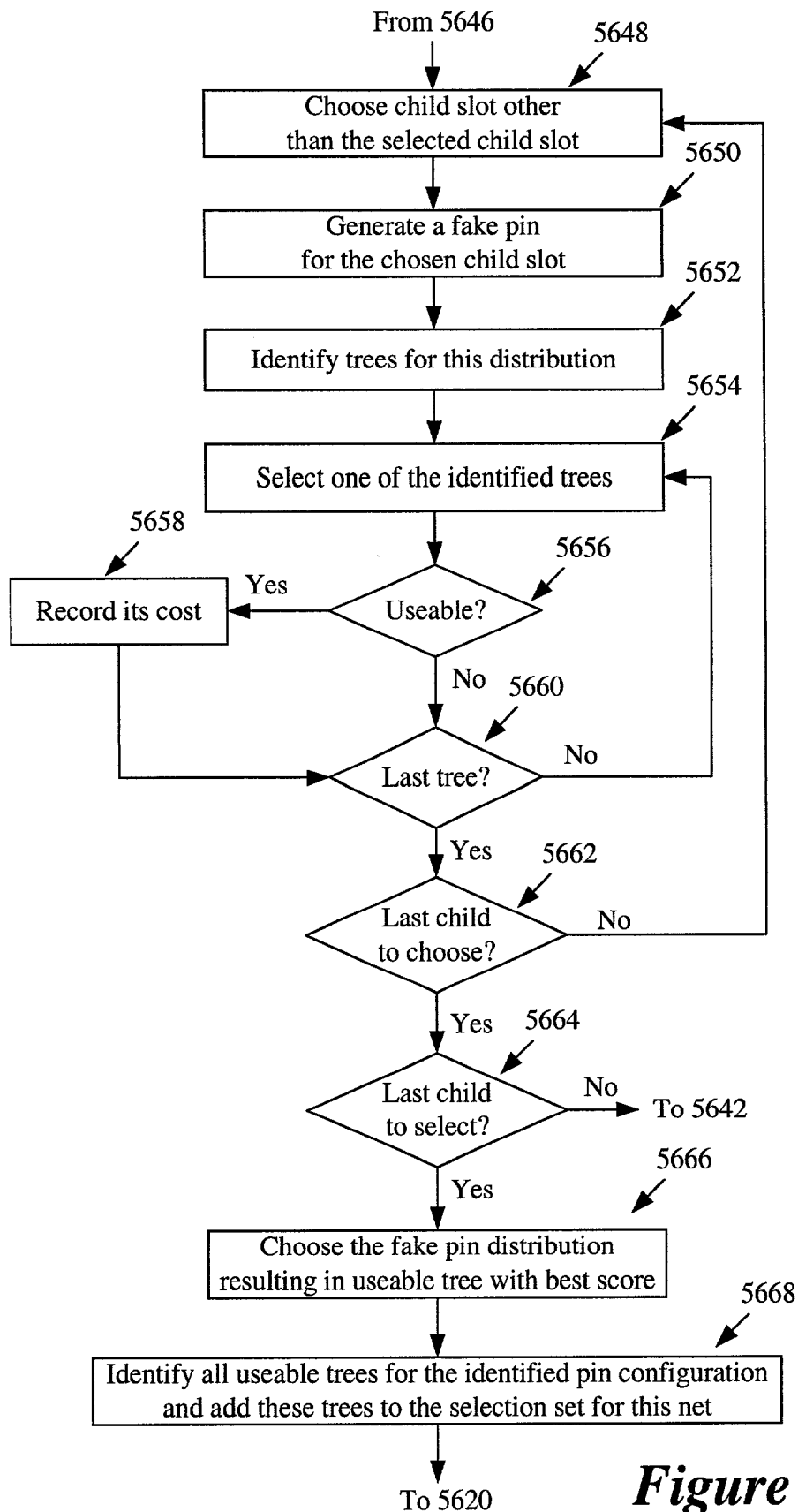


Figure 56D

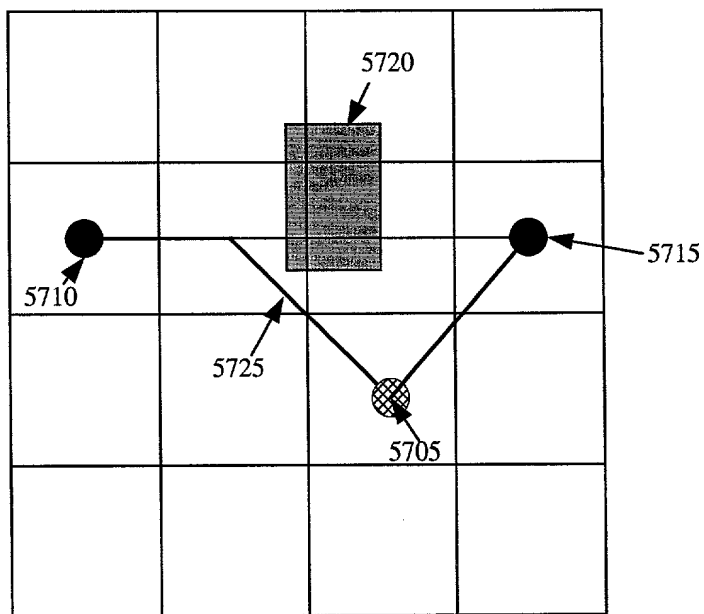


Figure 57

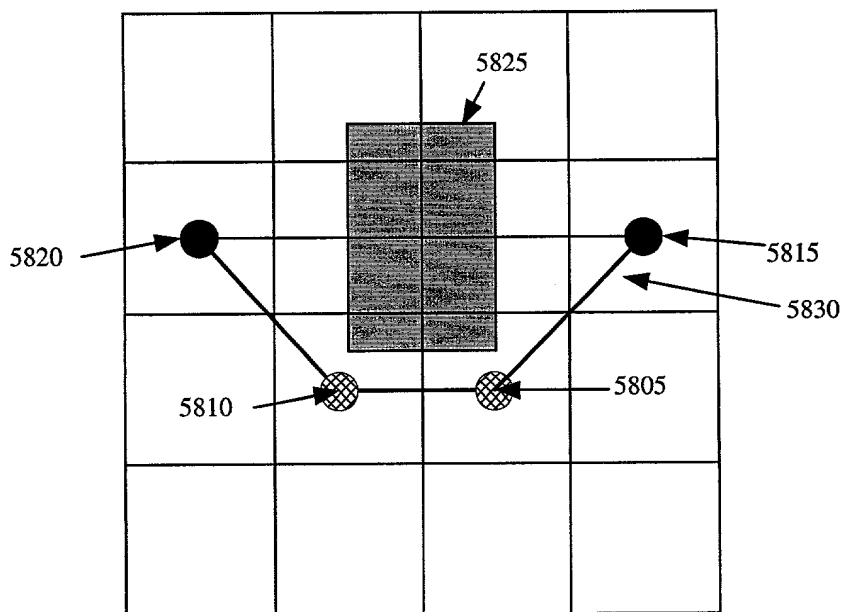


Figure 58

5915

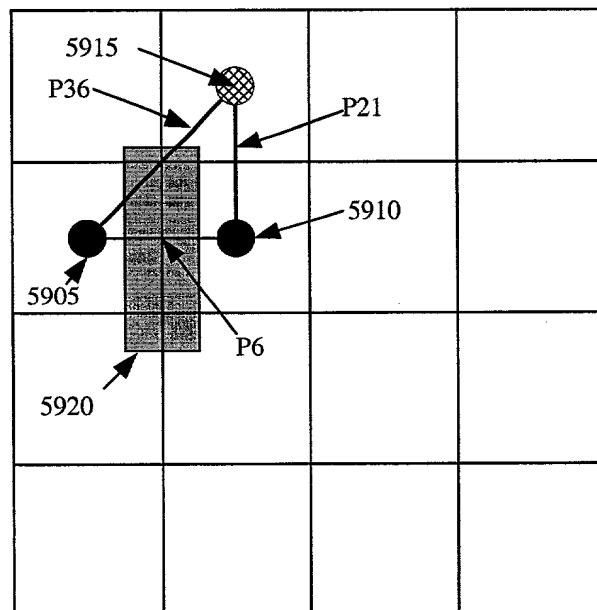


Figure 59

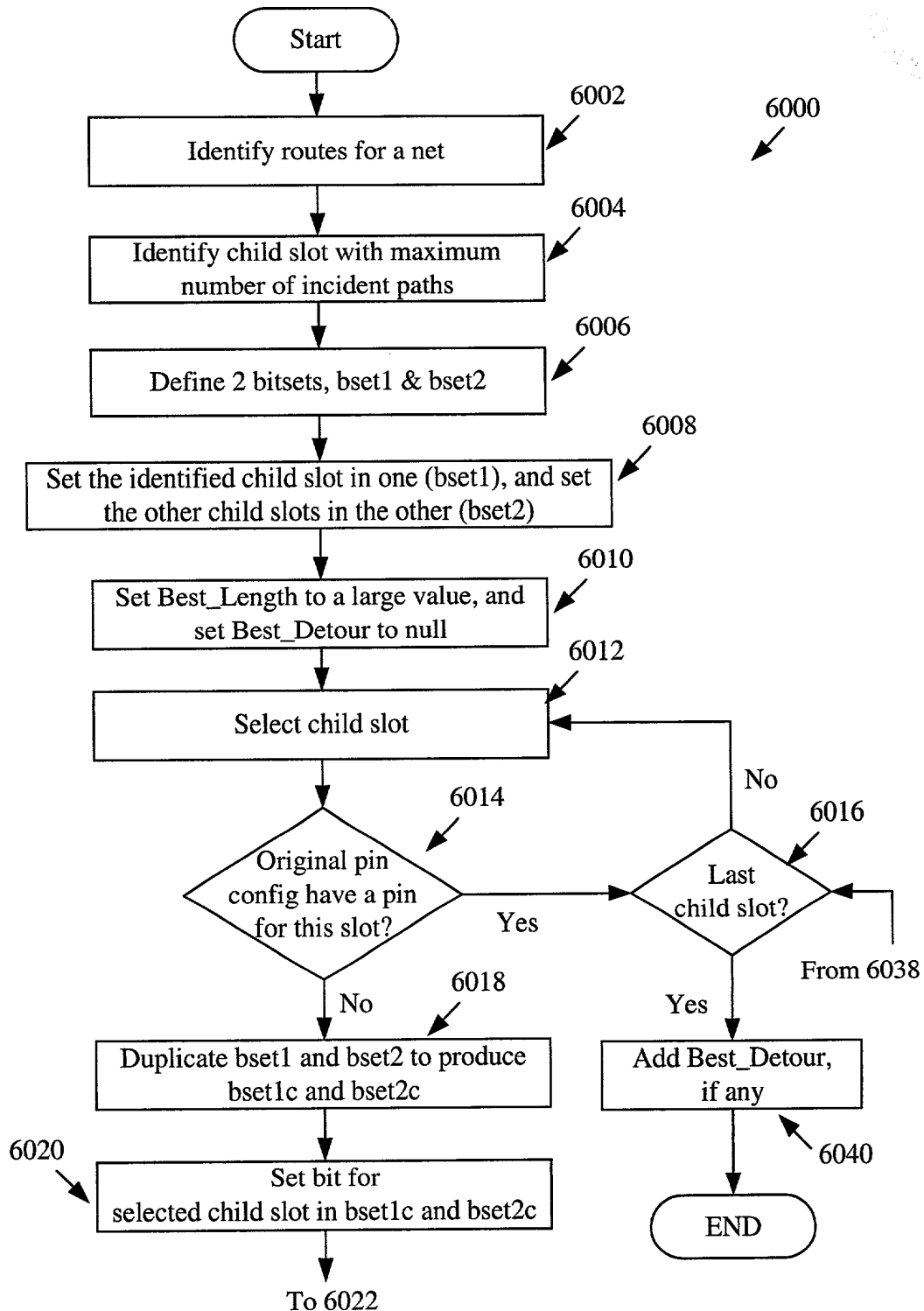


Figure 60A

**Figure 60: Figure 60A
Figure 60B**

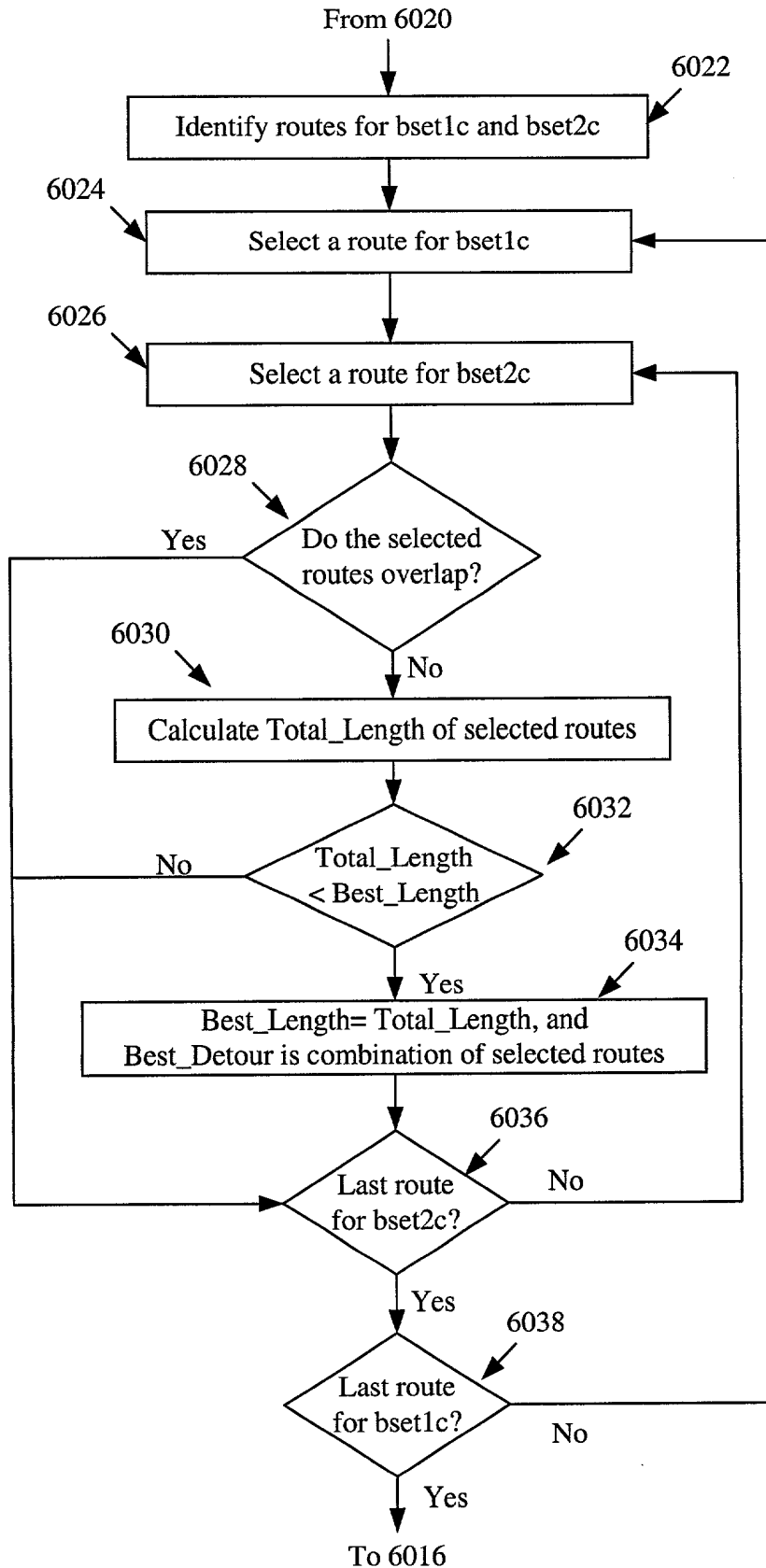


Figure 60B

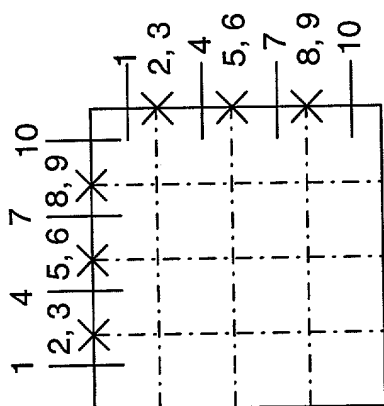


Figure 61

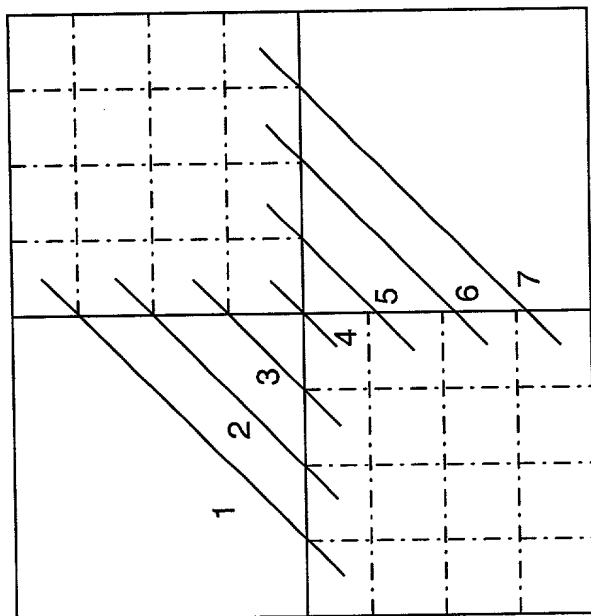


Figure 62

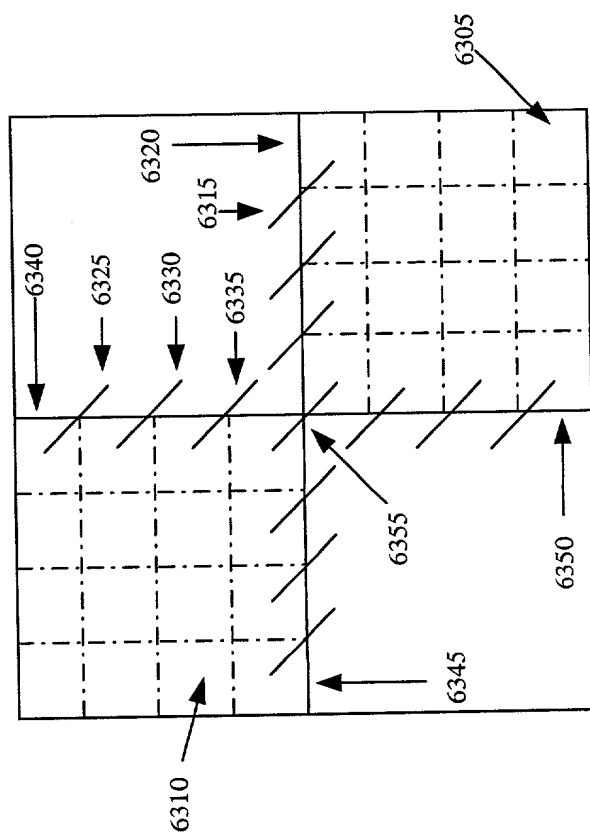


Figure 63

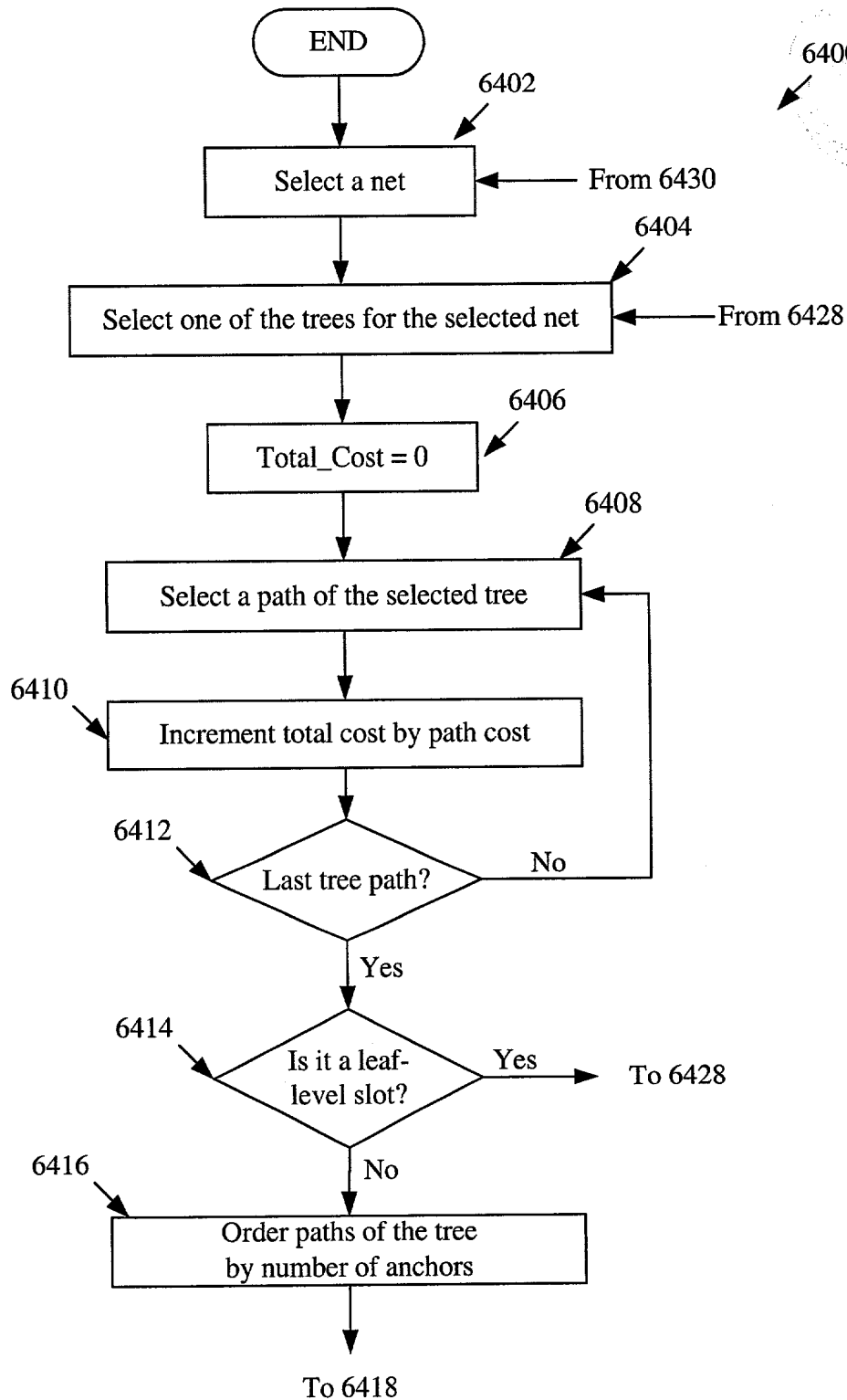


Figure 64A

Figure 64: Figure 64A
Figure 64B

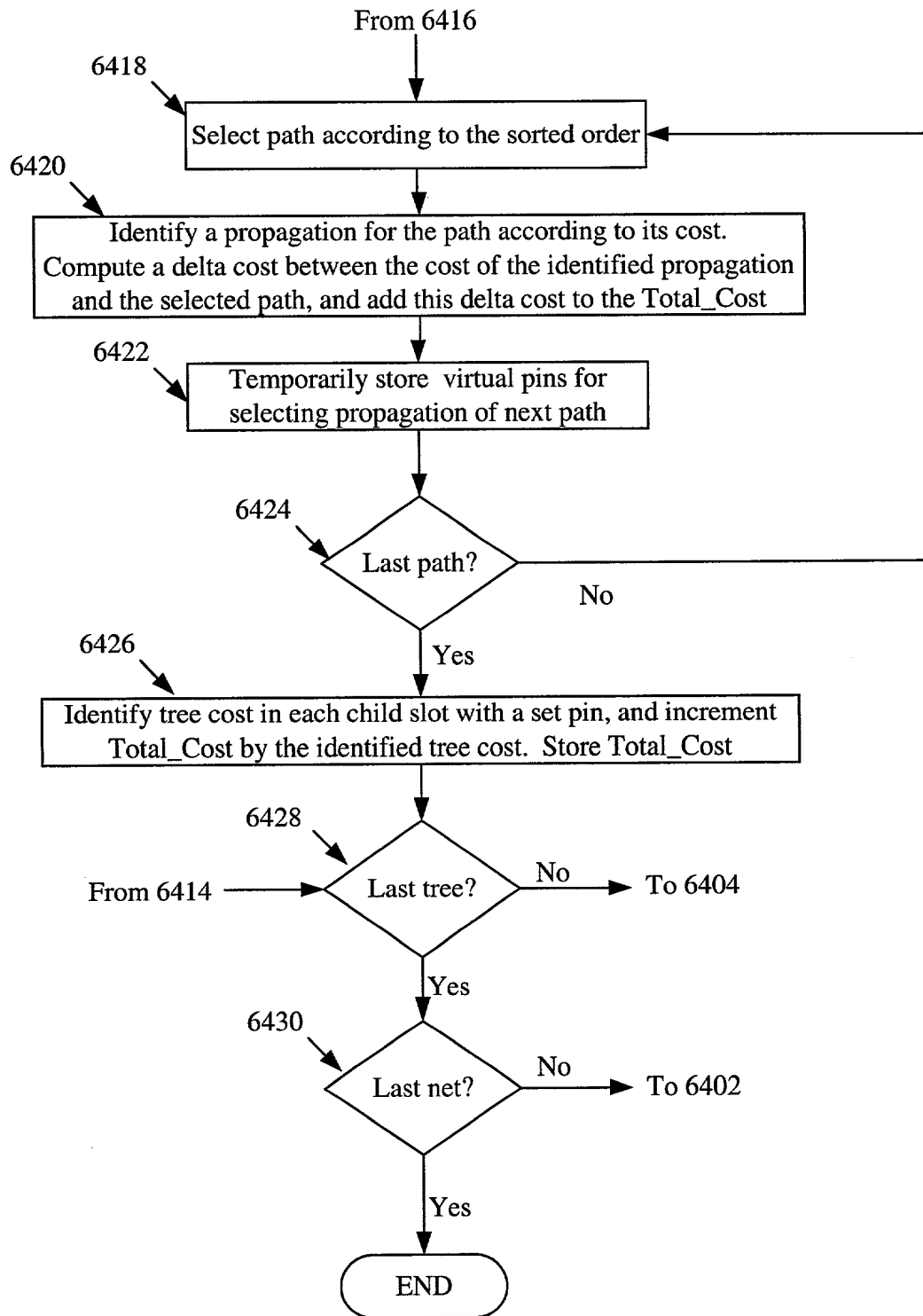


Figure 64B

FIG. 65 is a schematic diagram of a system for providing a user with a visual representation of a network topology. The system includes a network topology database 6500, a network topology processor 6510, and a network topology display 6520. The network topology processor 6510 is configured to receive network topology data from the network topology database 6500 and to process the data to generate a visual representation of the network topology. The network topology display 6520 is configured to display the visual representation of the network topology to the user.

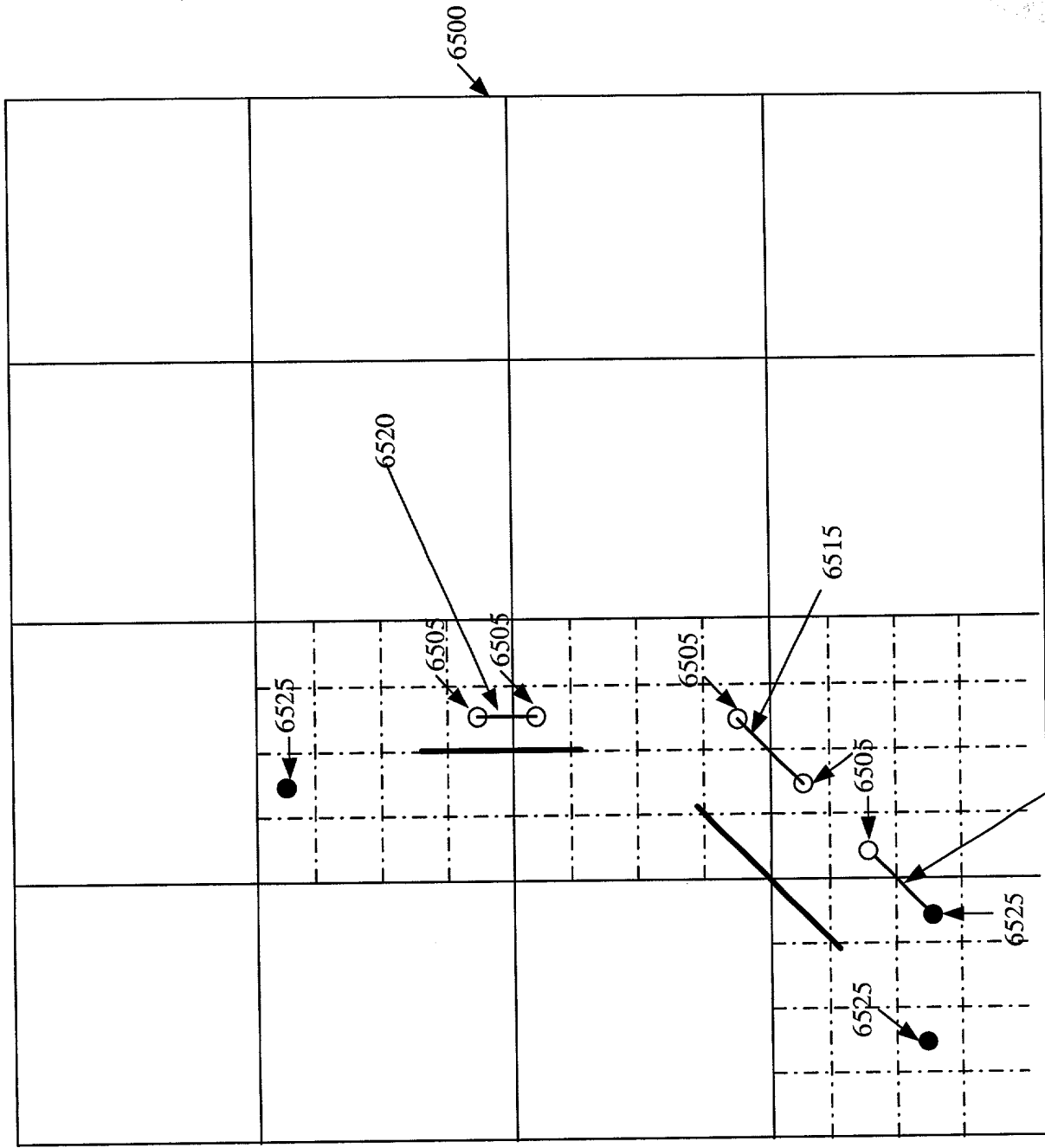


Figure 65

Figure 66

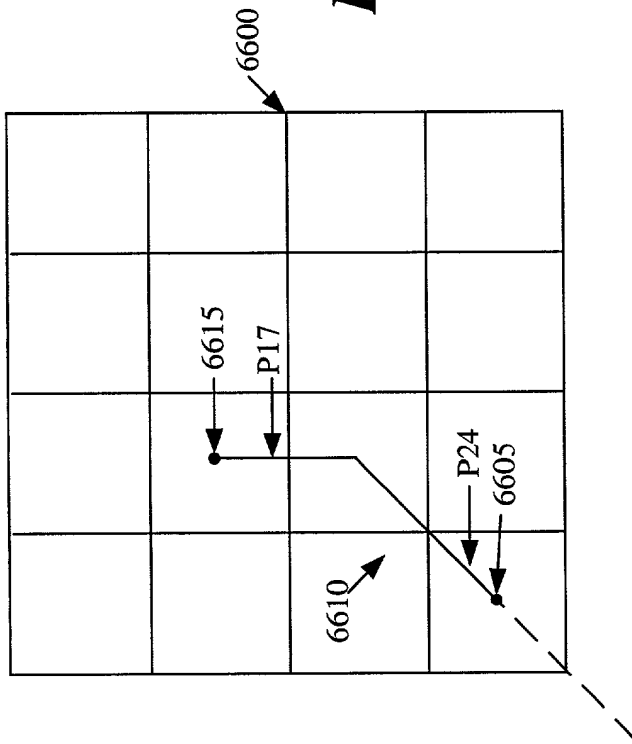
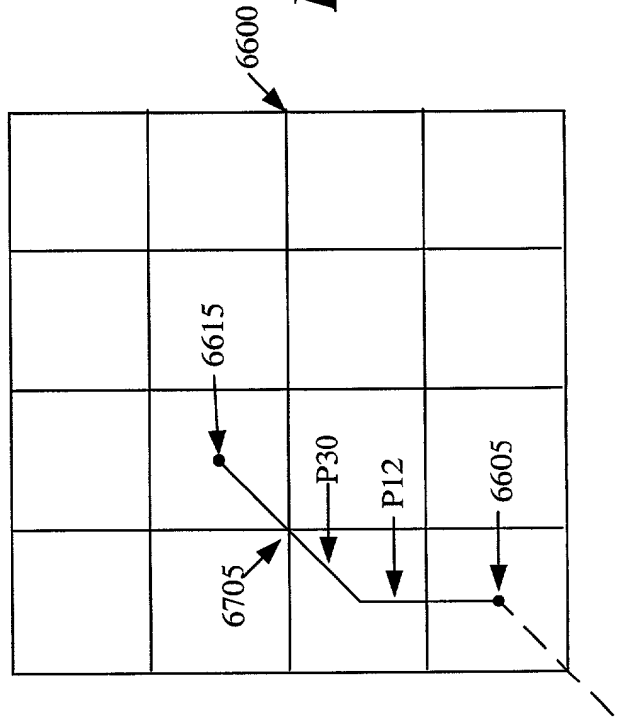


Figure 67



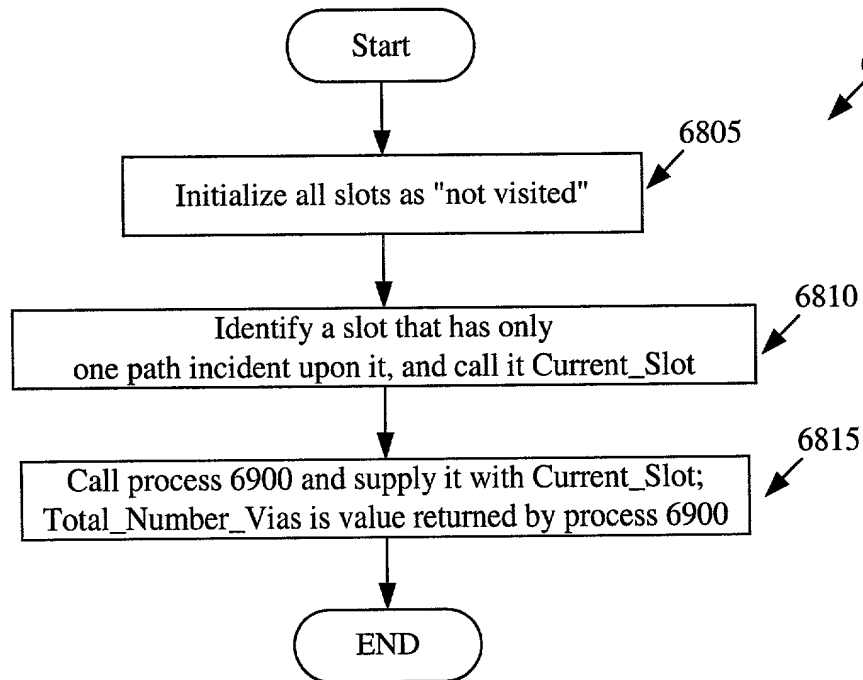


Figure 68

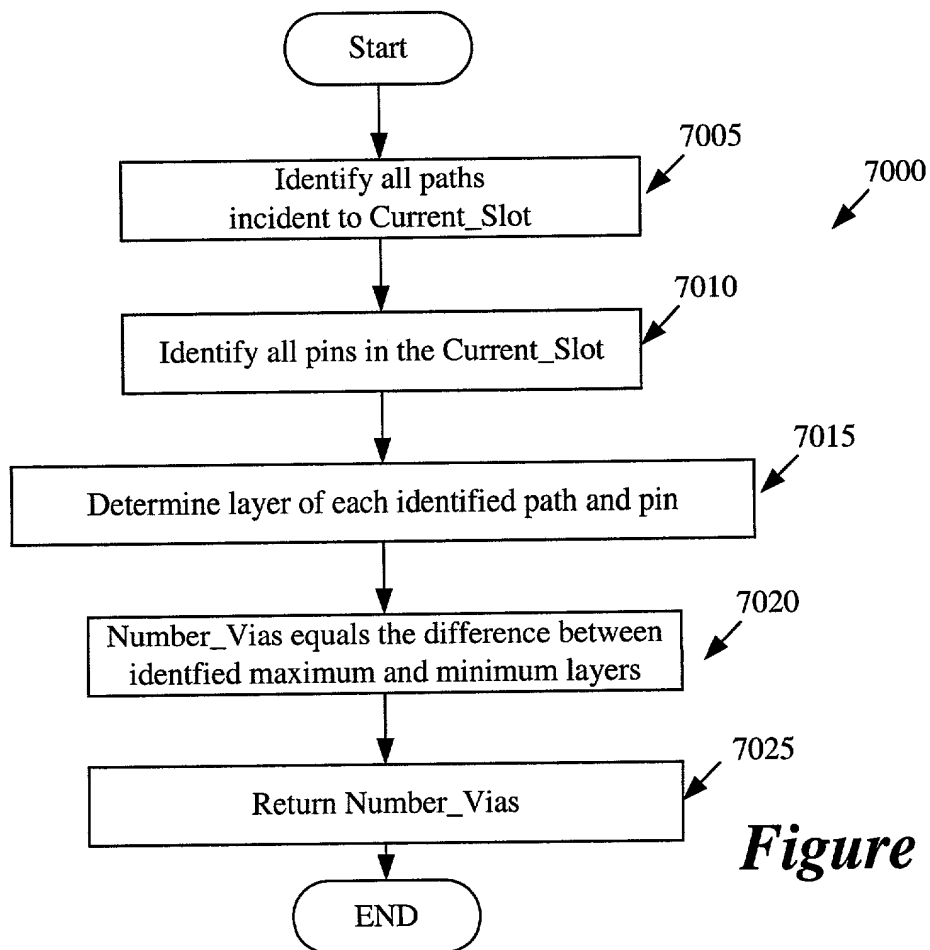


Figure 70

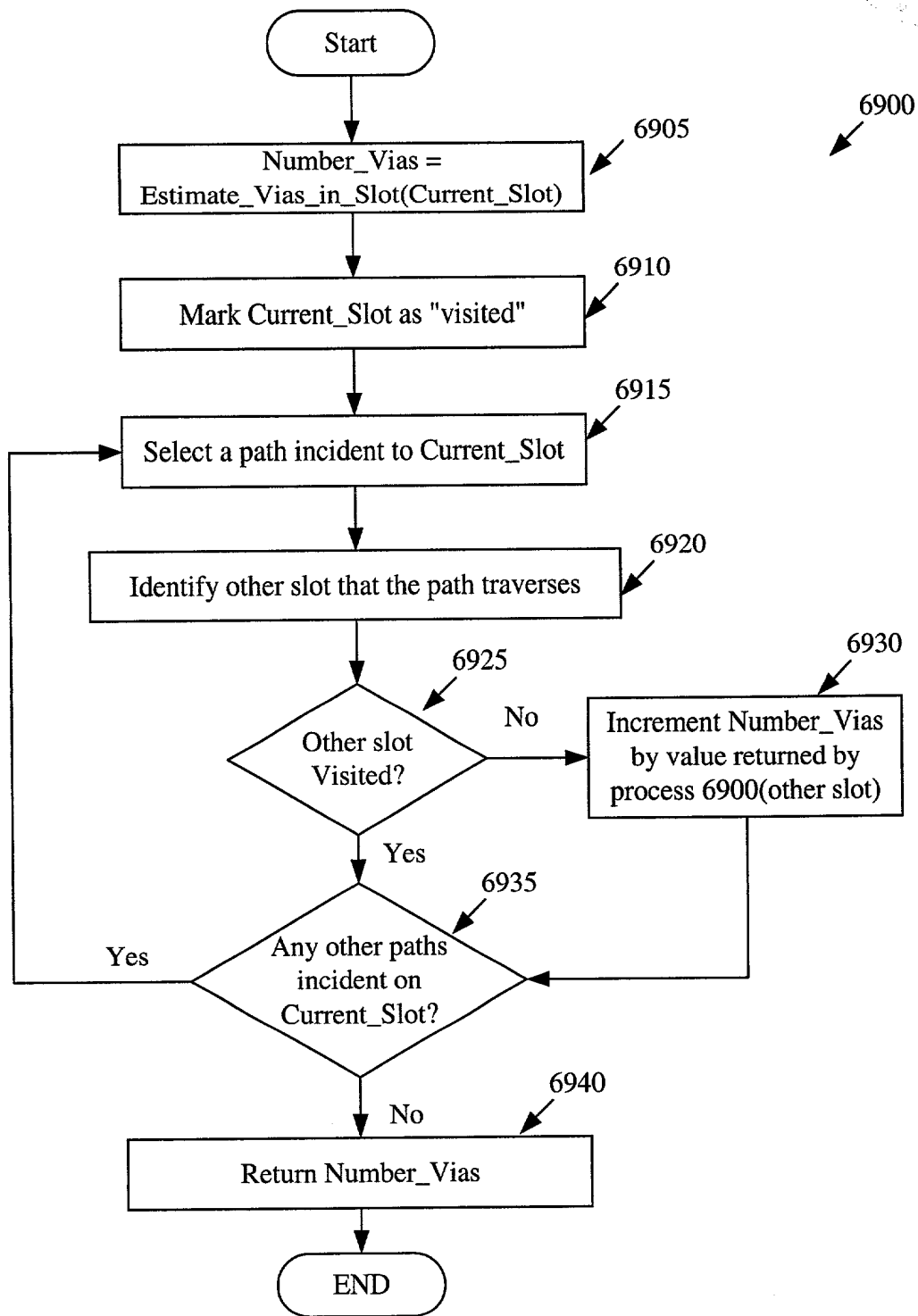


Figure 69

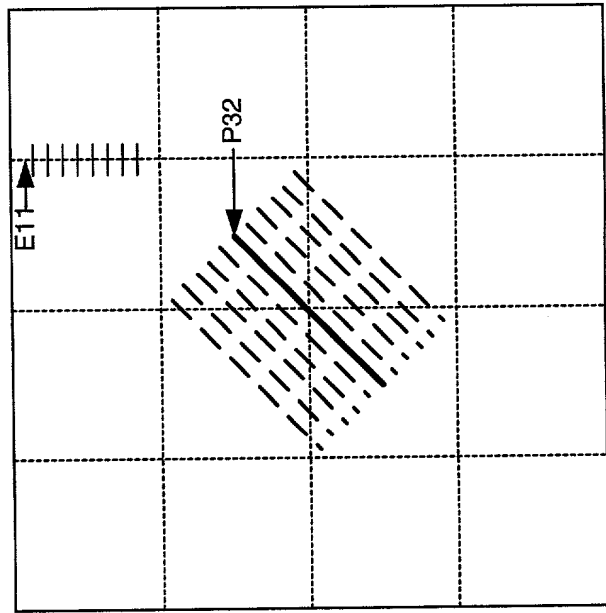


Figure 71

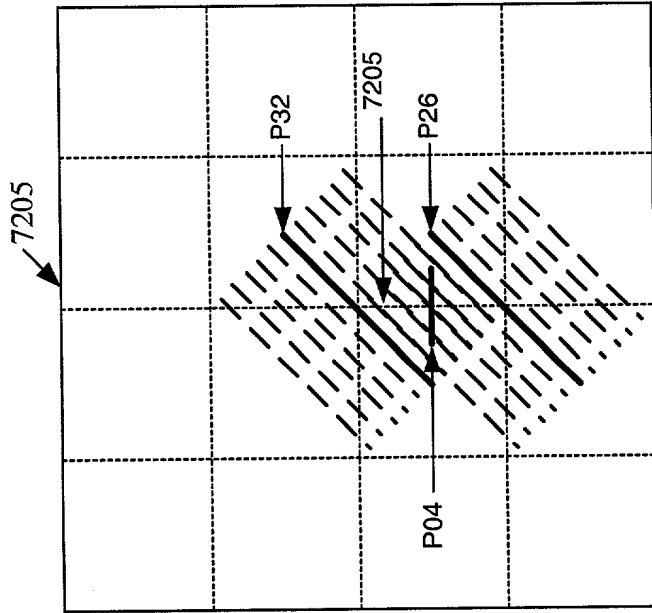


Figure 72

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1970	1971	1972	1973	1974	1975	1976	1977	1978	1979	1980	1981	1982	1983	1984	1985	1986	1987	1988	1989	1990	1991	1992	1993	1994	1995	1996	1997	1998	1999	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035	2036	2037	2038	2039	2040	2041	2042	2043	2044	2045	2046	2047	2048	2049	2050	2051	2052	2053	2054	2055	2056	2057	2058	2059	2060	2061	2062	2063	2064	2065	2066	2067	2068	2069	2070	2071	2072	2073	2074	2075	2076	2077	2078	2079	2080	2081	2082	2083	2084	2085	2086	2087	2088	2089	2090	2091	2092	2093	2094	2095	2096	2097	2098	2099	2100	

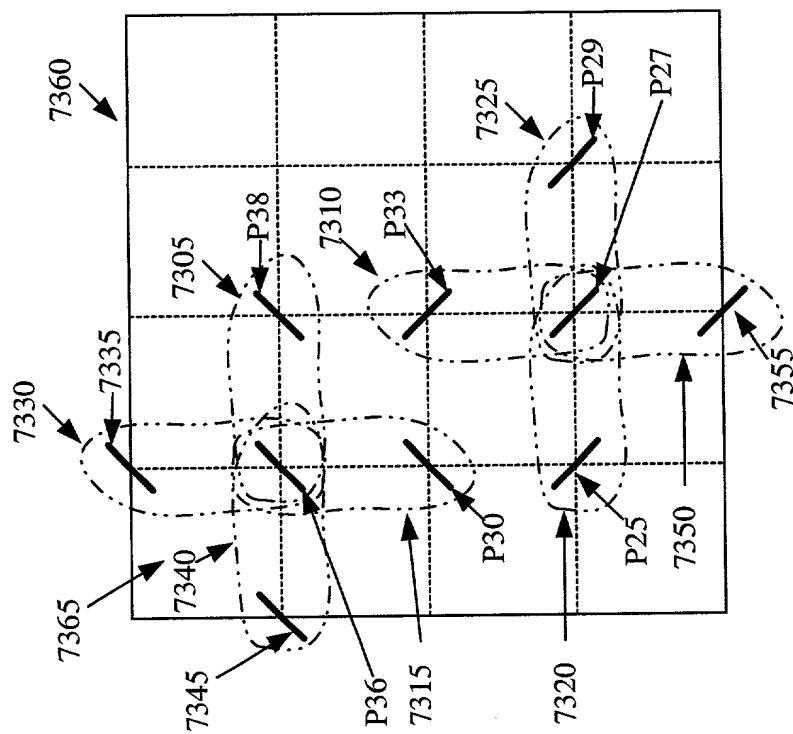


Figure 73

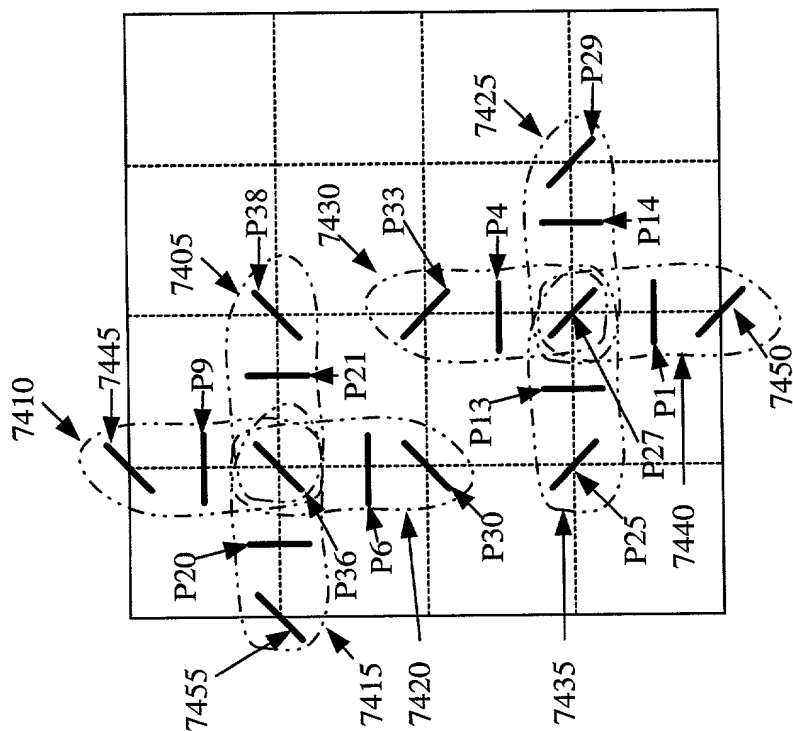


Figure 74

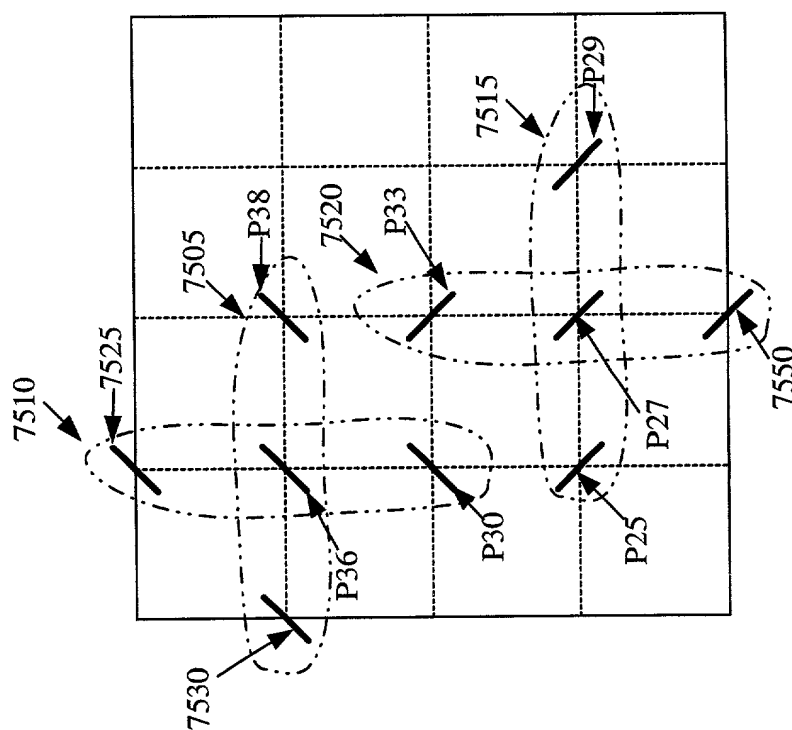


Figure 75

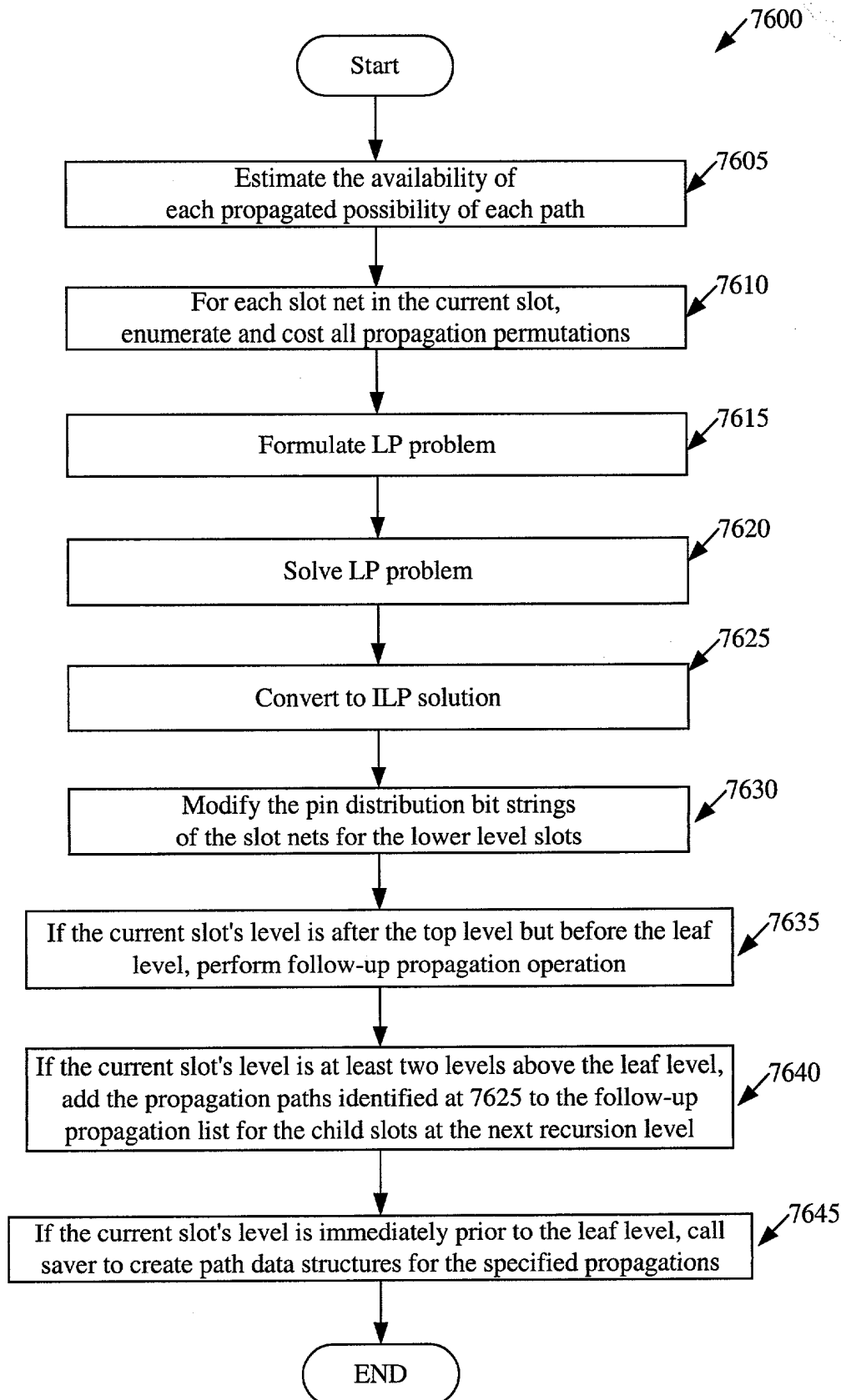


Figure 76

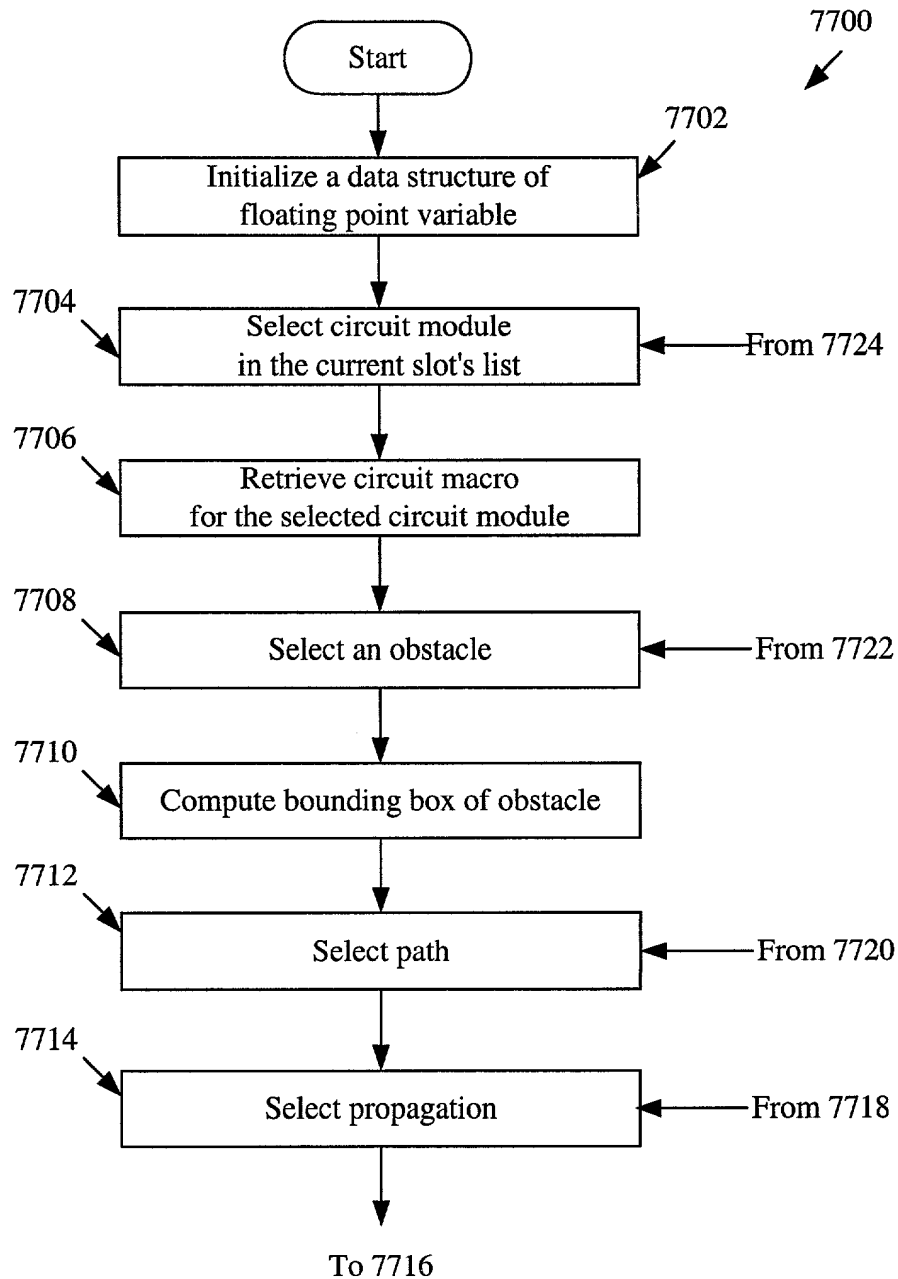


Figure 77A

Figure 77: $\frac{\text{Figure 77A}}{\text{Figure 77B}}$

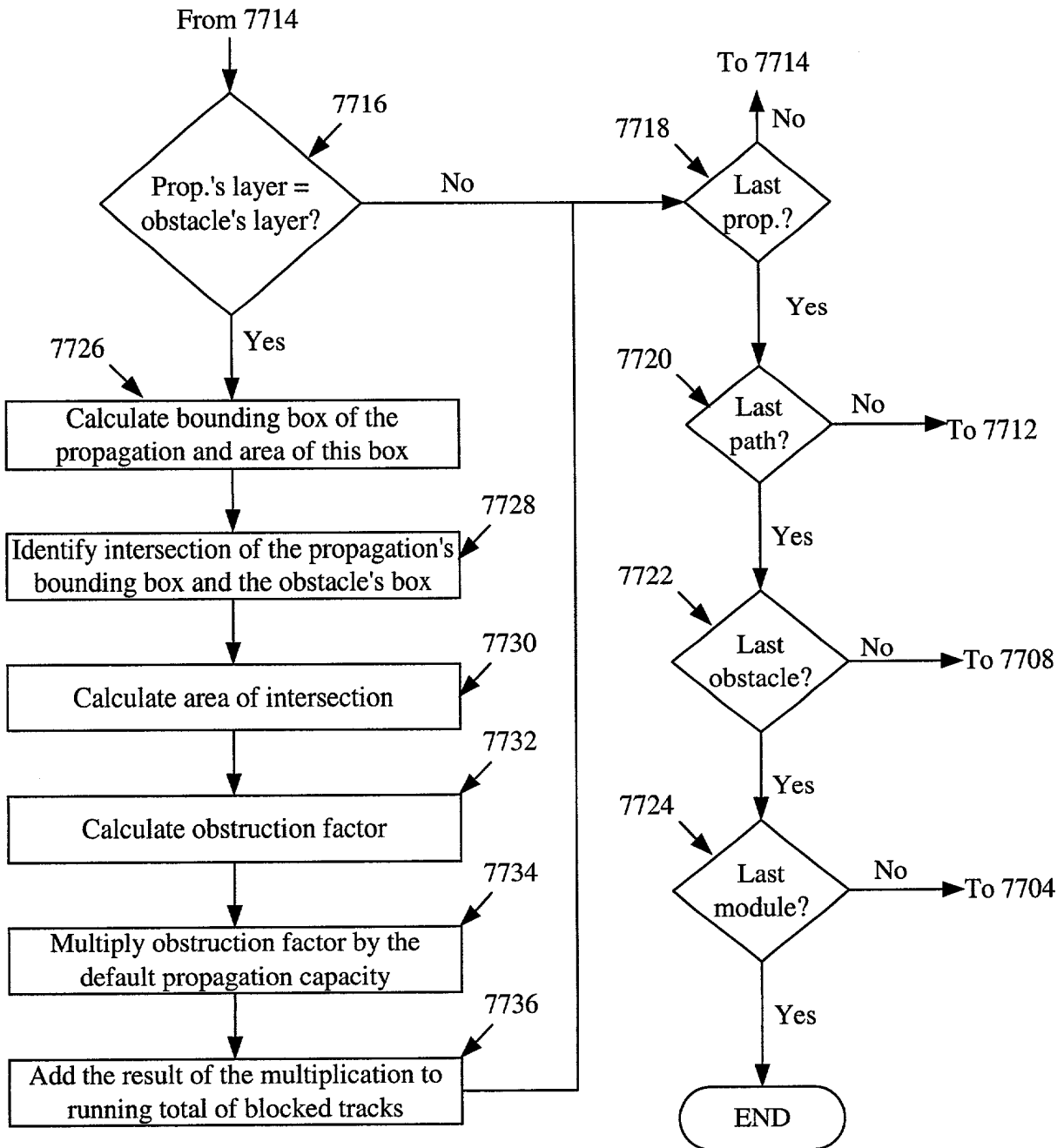


Figure 77B

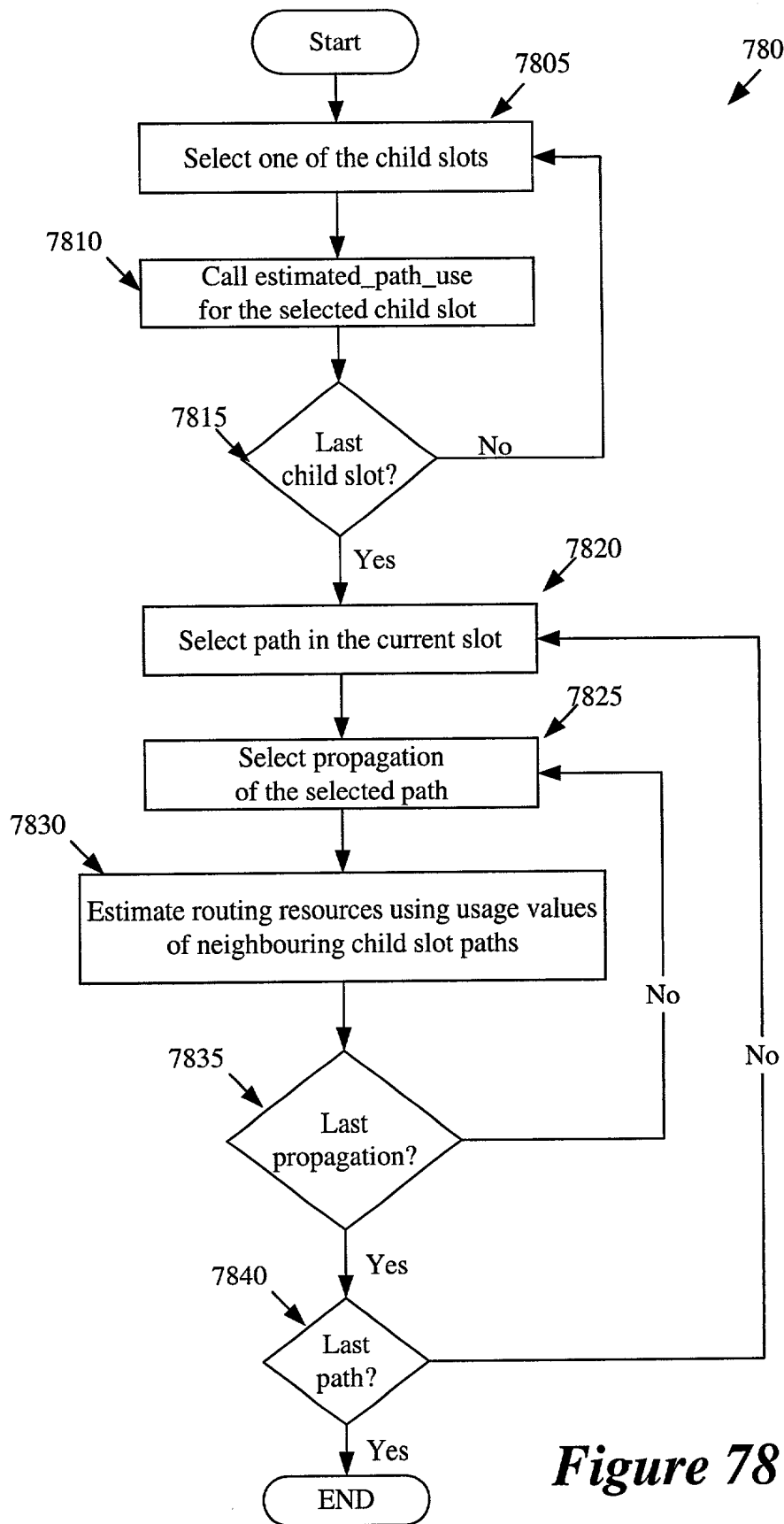


Figure 78

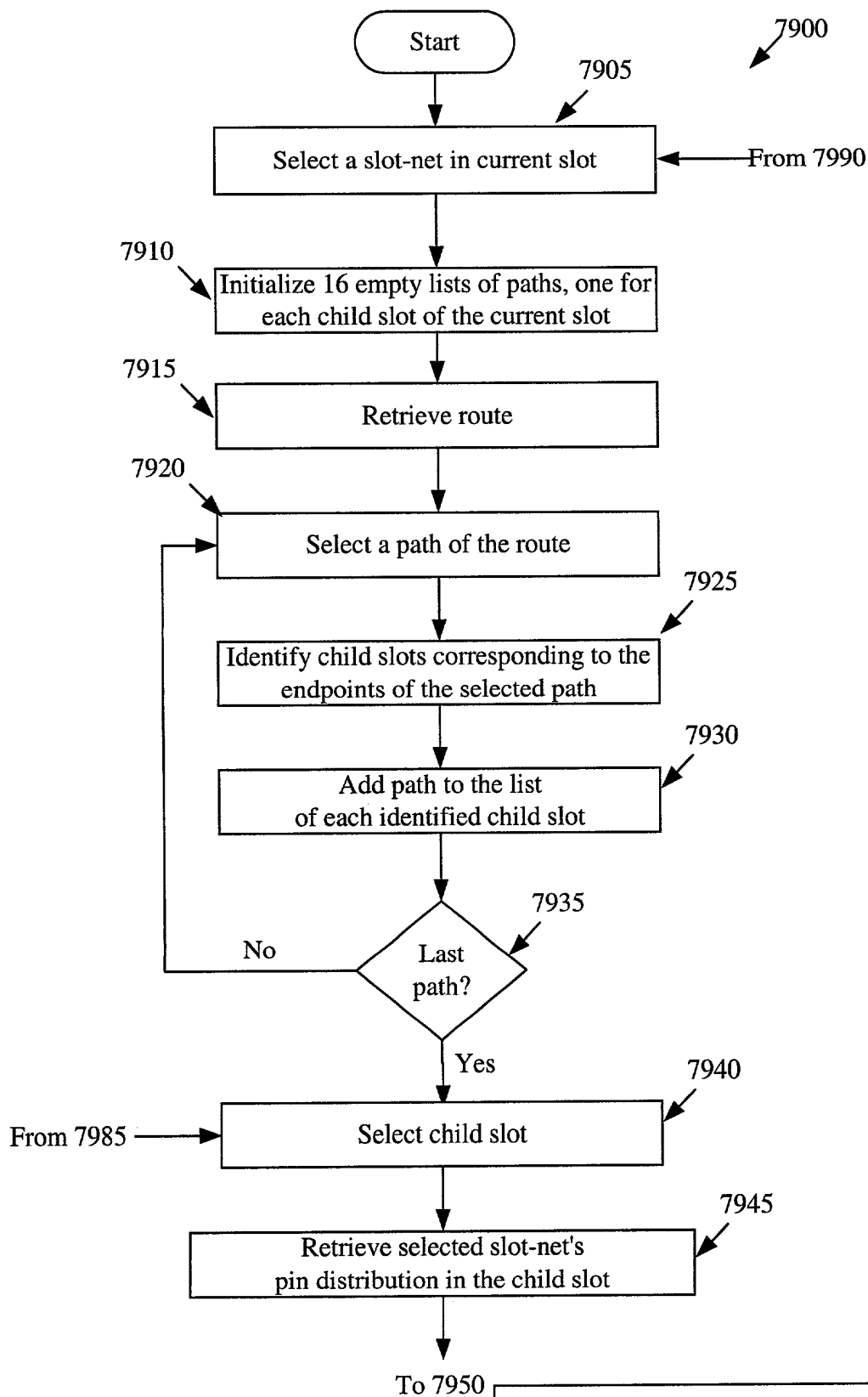


Figure 79A

**Figure 79: *Figure 79A*
*Figure 79B***

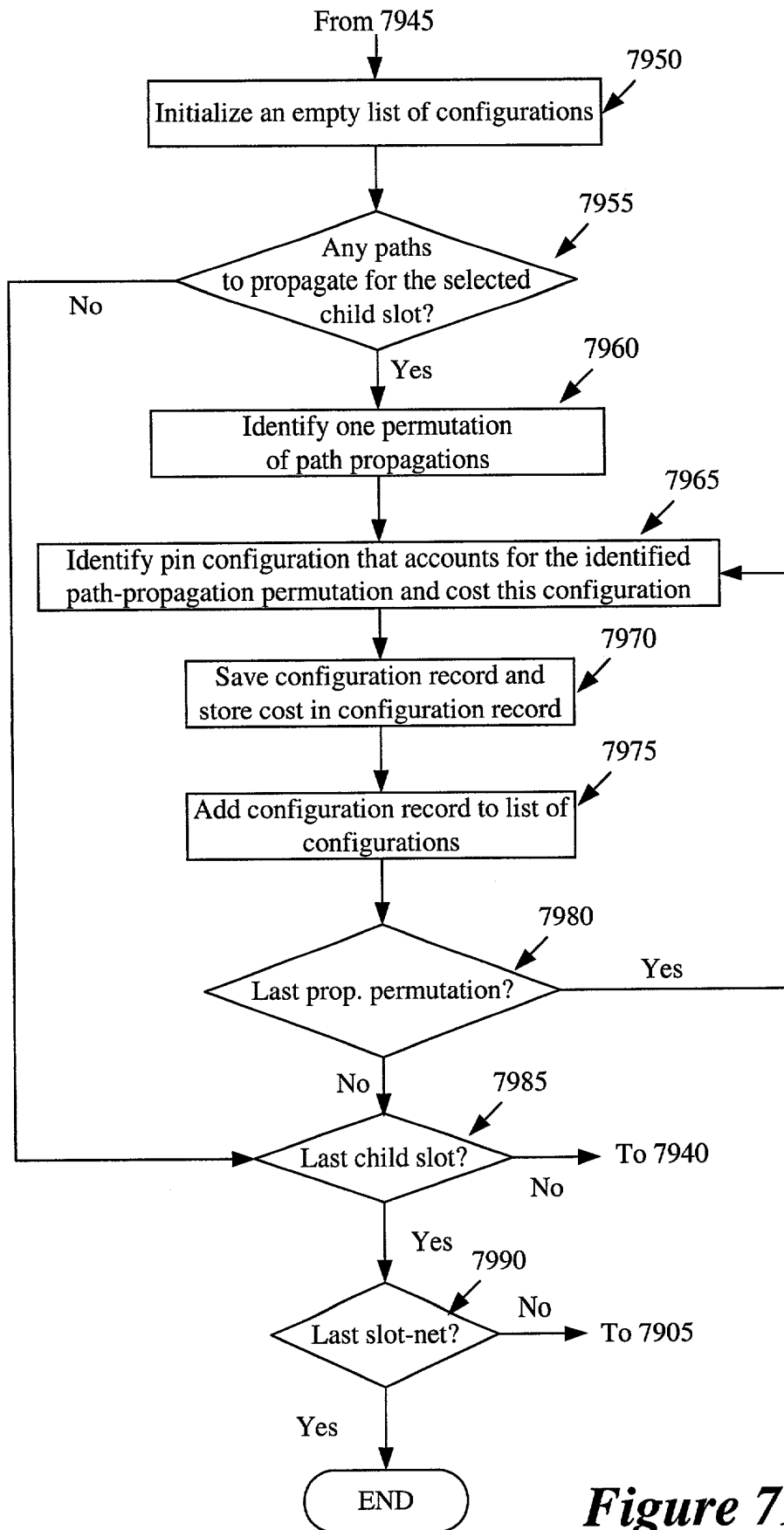
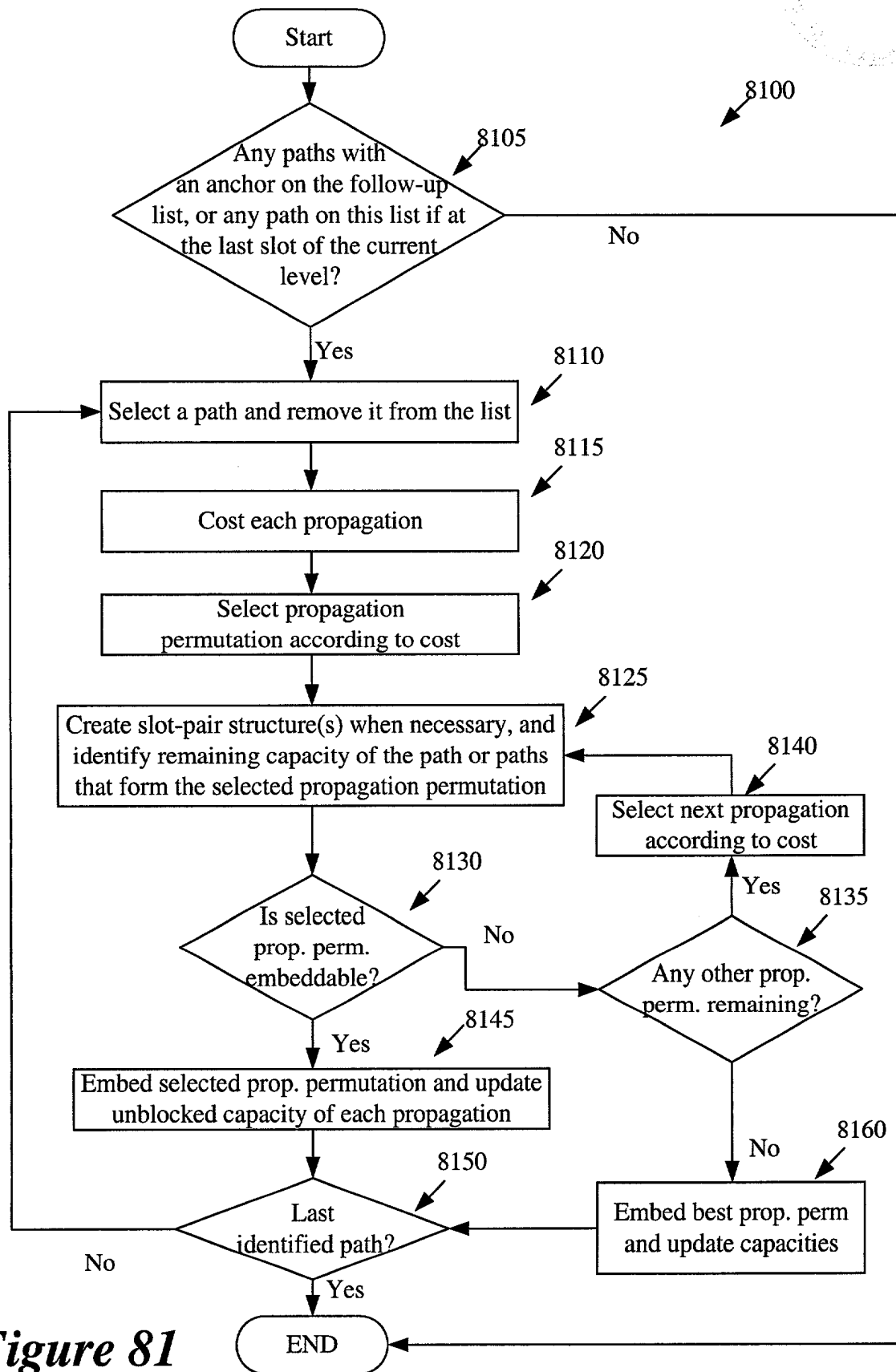


Figure 79B



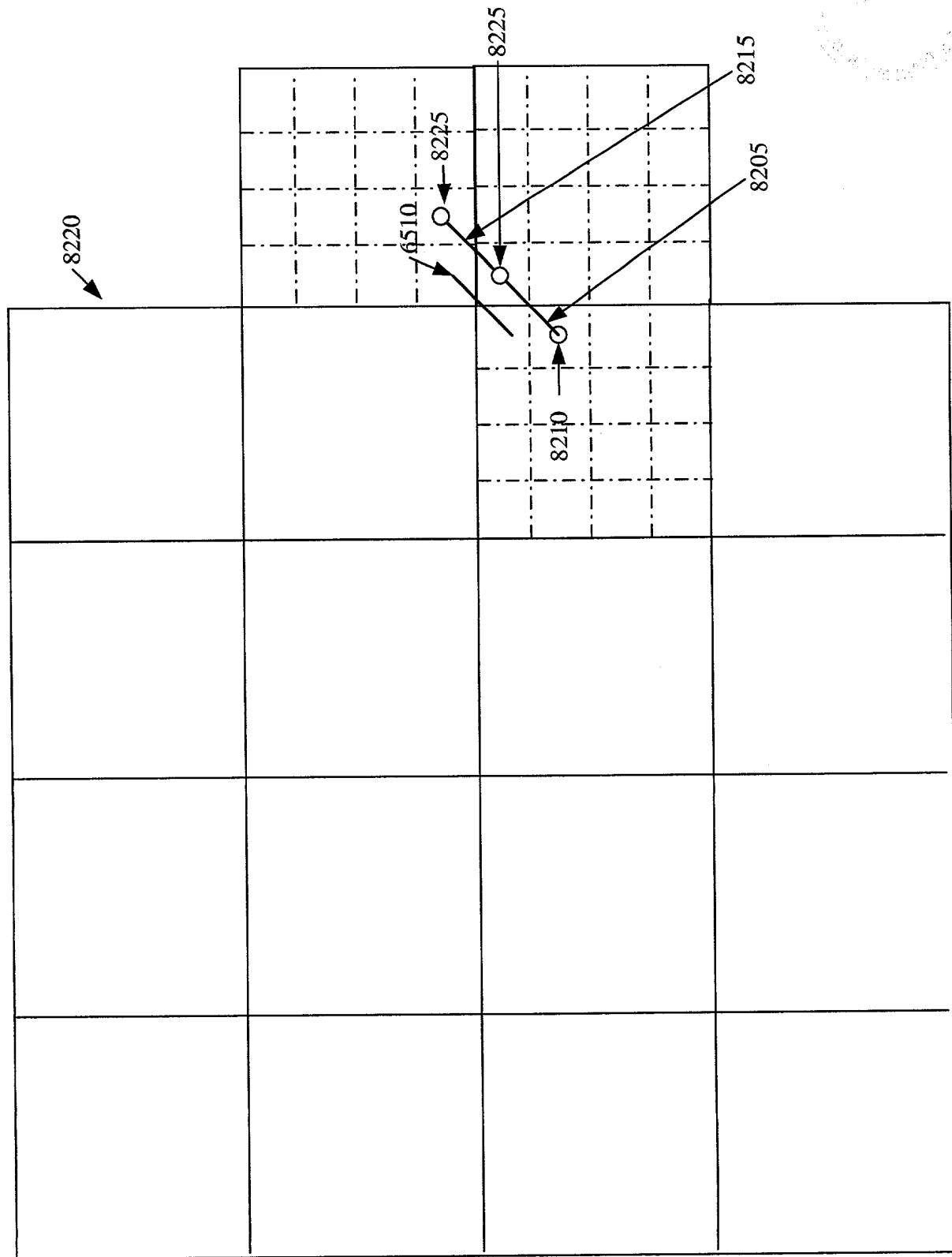


Figure 82

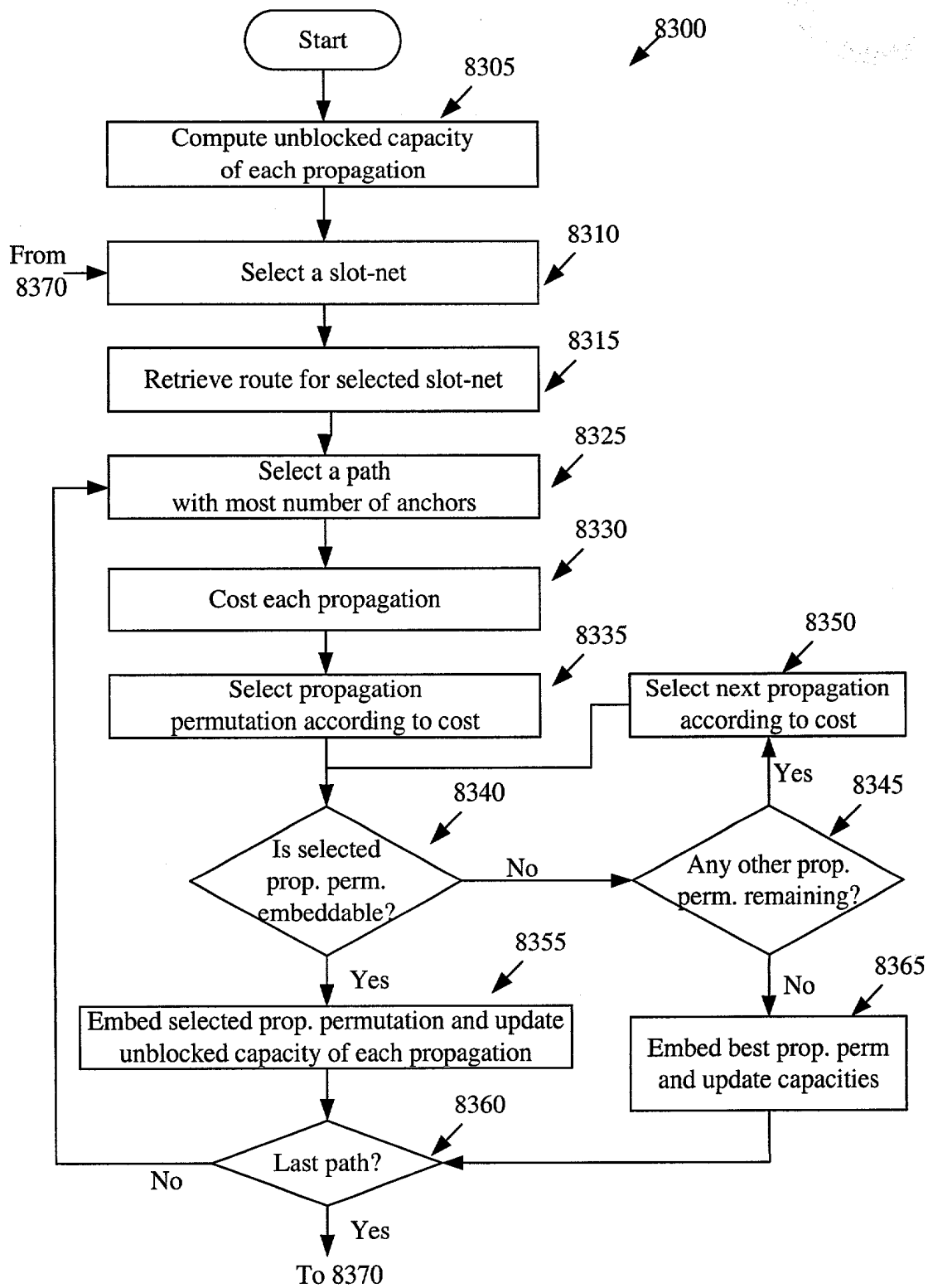


Figure 83A

Figure 83A
Figure 83B

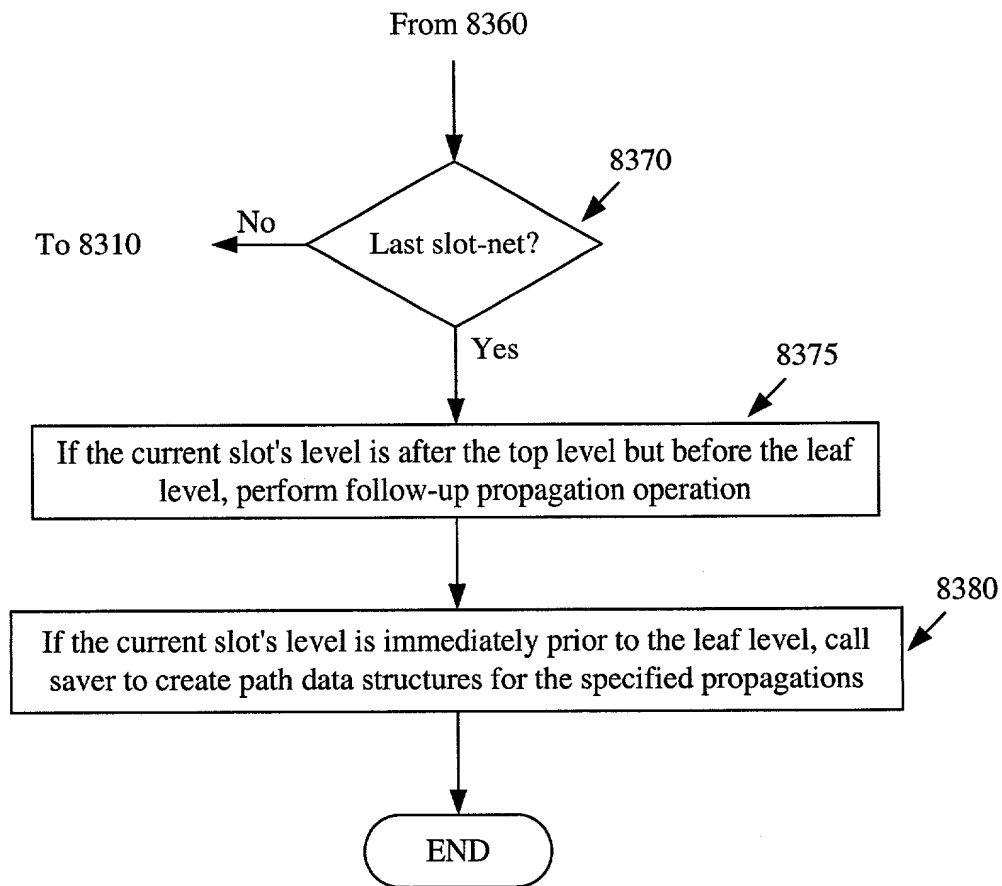


Figure 83B

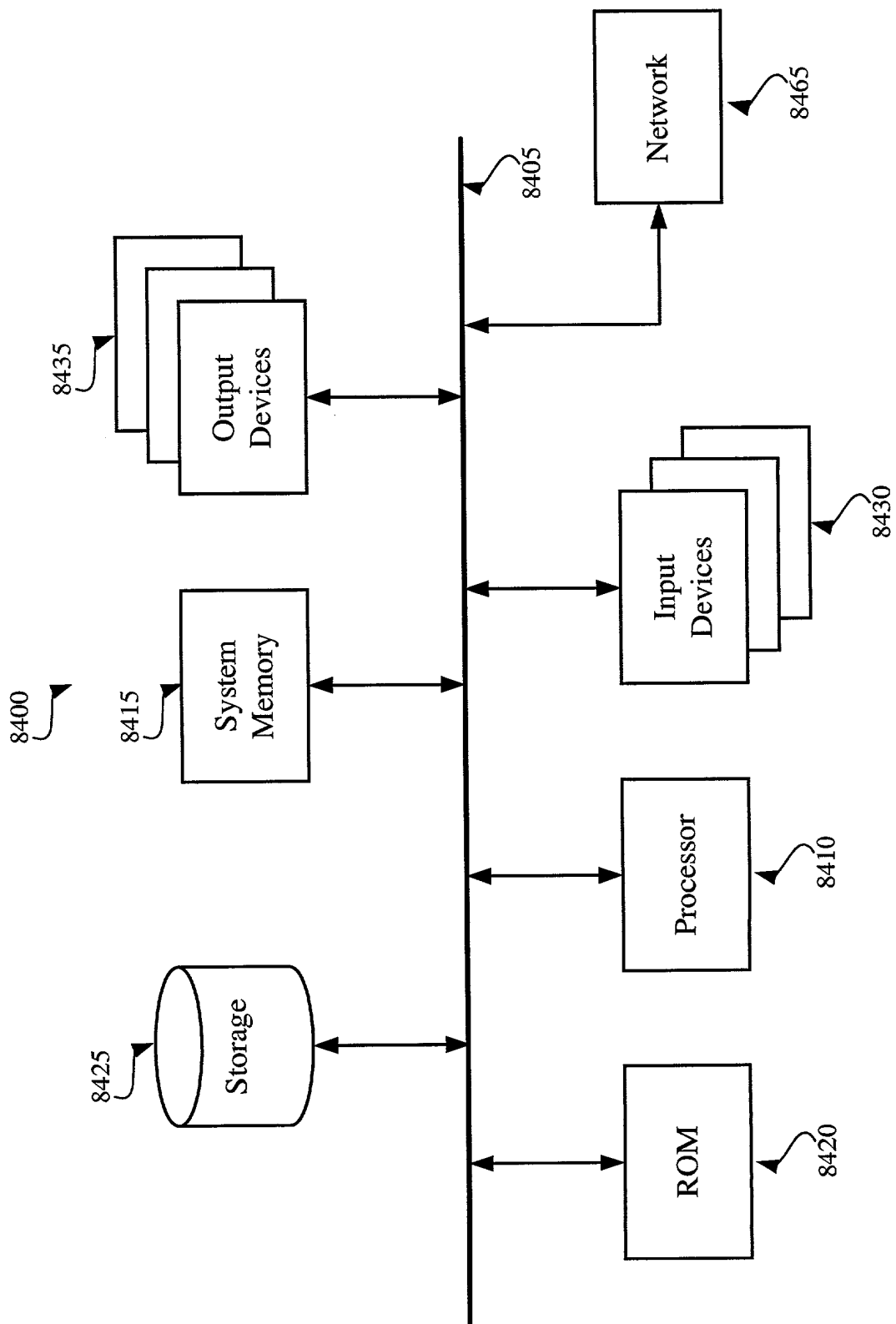


Figure 84